TEXAS INSTRUMENTS

TLK2501 Serdes EVM Kit Setup and Usage

User's Guide

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Mixed Signal Products

SLLU010

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Preface

Read This First

About This Manual

This manual should be used to determine how to setup and use the TLK2501 evaluation module in order to evaluate the TLK2501 device.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 — Introduction
- Chapter 2 — TLK2501 EVM Board Configuration
- Chapter 3 — PCB Construction and Characteristics
- Appendix A — Schematics, Board Layouts, and Suggested Optics and Cable Assembly Specifications
- Appendix B — NetLight™ 1417K4A 1300 nm Laser 2.5 Gbits/s SpeedBlaster™ Transceiver data sheet

Notational Conventions

This document uses the following conventions.

- Program listings, program examples, and interactive displays are shown in a `special typeface` similar to a typewriter's. Examples use a **`bold version`** of the special typeface for emphasis; interactive displays use a **`bold version`** of the special typeface to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

  Here is a sample program listing:

```
0011  0005  0001         .field    1, 2
0012  0005  0003         .field    3, 4
0013  0005  0006         .field    6, 3
0014  0006               .even
```

  Here is an example of a system prompt and a command that you might enter:

```
C:  csr –a /user/ti/simuboard/utilities
```

- In syntax descriptions, the instruction, command, or directive is in a **bold typeface** font and parameters are in an *italic typeface*. Portions of a syntax that are in **bold** should be entered as shown; portions of a syntax that are in *italics* describe the type of information that should be entered. Here is an example of a directive syntax:

  .asect **"***section name***",** *address*

  .asect is the directive. This directive has two parameters, indicated by *section name* and *address*. When you use .asect, the first parameter must be an actual section name, enclosed in double quotes; the second parameter must be an address.

- Square brackets (**[** and **]**) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets; you don't enter the brackets themselves. Here's an example of an instruction that has an optional parameter:

  LALK *16–bit constant [, shift]*

  The LALK instruction has two parameters. The first parameter, *16-bit constant*, is required. The second parameter, *shift*, is optional. As this syntax shows, if you use the optional second parameter, you must precede it with a comma.

  Square brackets are also used as part of the pathname specification for VMS pathnames; in this case, the brackets are actually part of the pathname (they are not optional).

- Braces ({ and }) indicate a list. The symbol **|** (read as *or*) separates items within the list. Here's an example of a list:

  ```
  { * | *+ | *– }
  ```

  This provides three choices: `*`, `*+`, or `*–`.

  Unless the list is enclosed in square brackets, you must choose one item from the list.

- Some directives can have a varying number of parameters. For example, the .byte directive can have up to 100 parameters. The syntax for this directive is:

  .byte $value_1$ *[, ... ,* $value_n$*]*

  This syntax shows that .byte must have at least one value parameter, but you have the option of supplying additional value parameters, separated by commas.

Trademarks

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Chapter 1

Introduction

The Texas Instruments (TI) TLK2501 serdes evaluation module (EVM) board is used to evaluate the TLK2501 device(VQFP) and associated optical interface (NetLight™) for point-to-point data transmission applications.

The board enables the designer to connect 50-Ω parallel buses to both transmitter and receiver connectors. The TLK2501, using high speed PLL technology, serializes, encodes (8b/10b) and transmits data along one differential pair. The receiver part of the device deserializes, decodes, and presents data on the parallel bus. The high speed (up to 2.5 Gbps) data lines interface to four 50-Ω controlled-impedance SMA connectors. The designer can either use this copper interface directly or loop back to the laser module section for an optical interface(not provided).

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1.1 Introduction

The TLK2501 EVM board can be used to evaluate device parameters while acting as a guide for high-speed board layout. The evaluation board can be used as a daughter board that is plugged into new or existing designs. Since the TLK2501 operates over a wide range of frequencies, designers need to optimize designs for the frequency of interest. Additionally, designers may wish to use buried transmission lines and provide additional noise attenuation and EMI suppression to optimize their end product.

As the frequency of operation increases, the board designer must take special care to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled to 50 Ω for both the high-speed differential serial and parallel data connections. In addition, impedance mismatches are reduced by designing the component pad size to be as close as possible to the width of the connecting transmission lines. Vias are minimized and, when necessary, placed as close as possible to the device drivers. Since the board contains both serial and parallel transmission lines, care was taken to control both impedance and trace length mismatch (board skew).

Overall, the board layout is designed and optimized to support high-speed operation. Thus, understanding impedance control and transmission line effects are crucial when designing high-speed boards.

Some of the advanced features offered by this board include:

- ❑ PCB (printed-circuit board) is designed for high-speed signal integrity.
- ❑ Flexibility–The PCB can be configured for copper or optical interfaces.
- ❑ SMA and parallel fixtures are easily connected to test equipment.
- ❑ All input/output signals are accessible for rapid prototyping.
- ❑ Analog and digital power planes can be supplied through separate banana jacks for isolation or can be combined using ferrite bridging networks.
- ❑ Series termination resistors provide parallel RD outputs.
- ❑ Onboard capacitors provide ac coupling of high-speed signals.

1.2 TLK2501 EVM Kit Contents

- ❑ TLK2501 EVM board
- ❑ TLK2501 EVM kit documentation (This document)

Chapter 2

TLK2501 EVM Board Configuration

The TLK2501 EVM board gives the developer various options for operation, many of which are jumper selectable. Other options can be either soldered into the EVM or connected through input connectors.

The TX and RX parallel connectors, J1–J4 of Figures 8 and 10 in Appendix A, provide a connection for both transmitted and received data. The reference clock is supplied through SMA connector J8, and jumper J5 must be installed between pins 1 and 2. A direct clock connection can also be made to the J5 pins 1 and 3. The high-speed serial data is transmitted through J13 and J14 SMA connectors. The received recovered clock (RX_CLK) is output through J15 header. Received data connects through SMA connectors J17 and J23 on the RX side of the board. Header J7 provides static signals (normally pulled high) to configure the device for different modes of operation. The J20 header indicates the optical transmitter has detected a signal, and J21 allows the operator to disable the optical transceiver.

The power planes are split three ways to provide power for different parts of the board. This prevents coupling of switching noise between the analog and digital sections of the TLK2501 and provides voltage isolation for the laser section. The laser section of the board requires 3.3 volts and is energized through the VCC connector. The VDD and VDDA connectors require 2.5 volts and are joined together by a removable ferrite bead L3 that is installed in the default configuration. Thus, only the VDD connection is necessary to energize the TLK2501 device in the default configuration. In all sections of the board, the ground planes are common and each ground plane is tied together at every component ground connection. For detail schematic and layout see *TLK2501EVM Schematic*, *Optical Transceiver Schematic* and *Board Layer Stack–up* in Appendix A.

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The board is normally delivered in a default configuration that requires external clock and data inputs. The TLK2501 is shipped with jumpers for default operation. Table 2–1 shows the default configuration for sending data.

Table 2–1. Default Transceiver Board Configuration as Shipped

Designator	Function	Condition
J5	GTX CLK SEL	Jumper installed: J5 provides a method of supplying a input clock to the board
J7	TESTEN	Jumper installed (Logic 0) Disables the TLK2501 test mode
J7	PRBSEN	Jumper installed (Logic 0) Disables the TLK2501 PRBS internal production test mode
J7	LCKREFN	Jumper not installed (Logical 1) Locks to received clock
J7	ENABLE	Jumper not installed (Logical 1) Enables the device for normal operation
J7	TXER	Jumper installed (Logic 0) Puts the TLK2501 in a state to transmit TX bus data.
J7	LOOPEN	Jumper installed (Logic 0) Disables the TLK2501 internal loop back mode
J7	TXEN	Jumper not installed (Logical 1) Puts the TLK2501 in a state to transmit TX bus data
L3	VDD– bridge –VDDA	Joins VDD and VDDA power planes
C24, C25	TX ac coupling capacitors	These capacitors (normally installed) are provided to ac-couple the transmitted signal.
C22, C23	RX ac coupling capacitors	These capacitors (normally installed) are provided to ac-couple the received signal

Note: For details, see TLK2501 data sheet

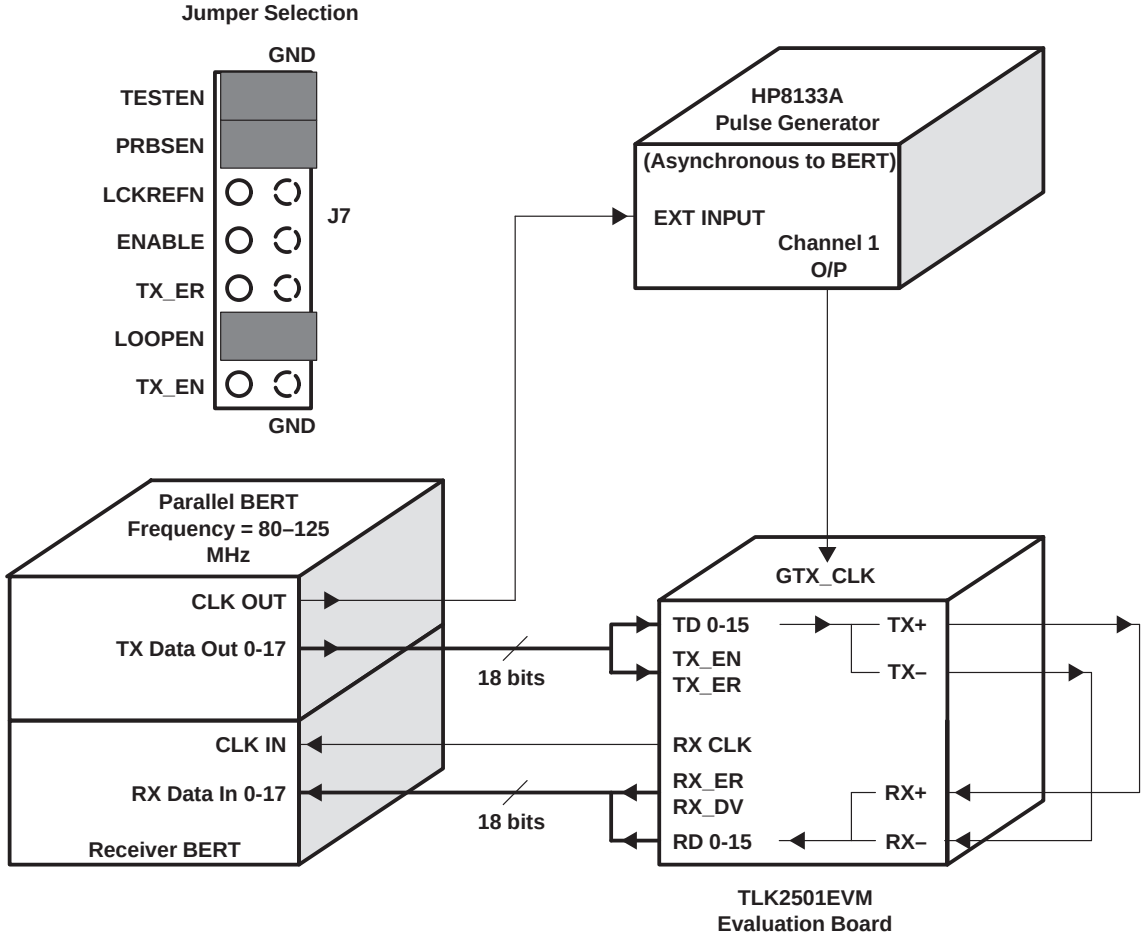
Table 2–2. Configuration Changes Necessary for DC-Coupling of the High Speed Signals

Designator	Function	Condition or Changes Necessary for DC Coupling
C24, C25	TX ac coupling capacitors	Install zero ohm resistors
C22, C23	TX ac coupling capacitors	Install zero ohm resistors.
R34	RX bias resistor	Install zero ohm resistor.
R33	RX bias resistor	Uninstall resistor (open circuit)
R37, R38	TX termination network	Uninstall resistors (open circuit): Termination and pullup is achieved at the receiver. Differential swing is increased.

2.1 Typical Test and Setup Configurations

The following configurations are used to evaluate and test the TLK2501 transceiver. The first configuration is a serial loopback of the high-speed signals shown in Figure 2–1. The serial loopback allows the designer to evaluate most of the functions of both transmitter and receiver sections of the TLK2501 device. To test a system, a parallel bit error rate tester (BERT) generates a predefined parallel bit pattern. The pattern is connected to the transmitter through parallel connectors TD0–TD15. Additionally, two control pins TX_ER and TX_EN are configured by the BERT for valid data transmission (TX_ER low and TX_EN high). The TLK2501 device encodes, serializes and presents the data on the high-speed serial pair. The serial TX data is then looped back to the receiver side and the device deserializes, decodes and presents the data on the receive side RD0–RD15. The data and indication bits (RX_DV and RX_ER) are received by the BERT and compared against the transmitted pattern and monitored for valid data and errors. If any bit errors are received, a bit error rate is evaluated at the parallel receive BERT.

Figure 2–1. TLK2501 Serial Loop-Back Test Configuration



If a parallel BERT is not available, the designer can take advantage of the built in test mode of the device, see Figure 2–2. If the designer asserts the PRBSEN pin high this results in a pseudo random bit pattern to be transmitted. This pin also puts the receiver in a mode to detect a valid PRBS pattern. A valid pattern is indicated by the PRBSPASS pin indicating high. This test only validates the high-speed serial portion of the device and system interconnects. The PRBS pattern is compatible with most serial BERT test equipment. This function allows the operator to isolate and test the transmitter and receiver independently. A typical configuration is shown in Figure 2–3. The dashed lines represent optional connections that can be made monitoring eye patterns and measuring jitter.

Figure 2–2. TLK2501 Serial Loop-Back Test Configuration

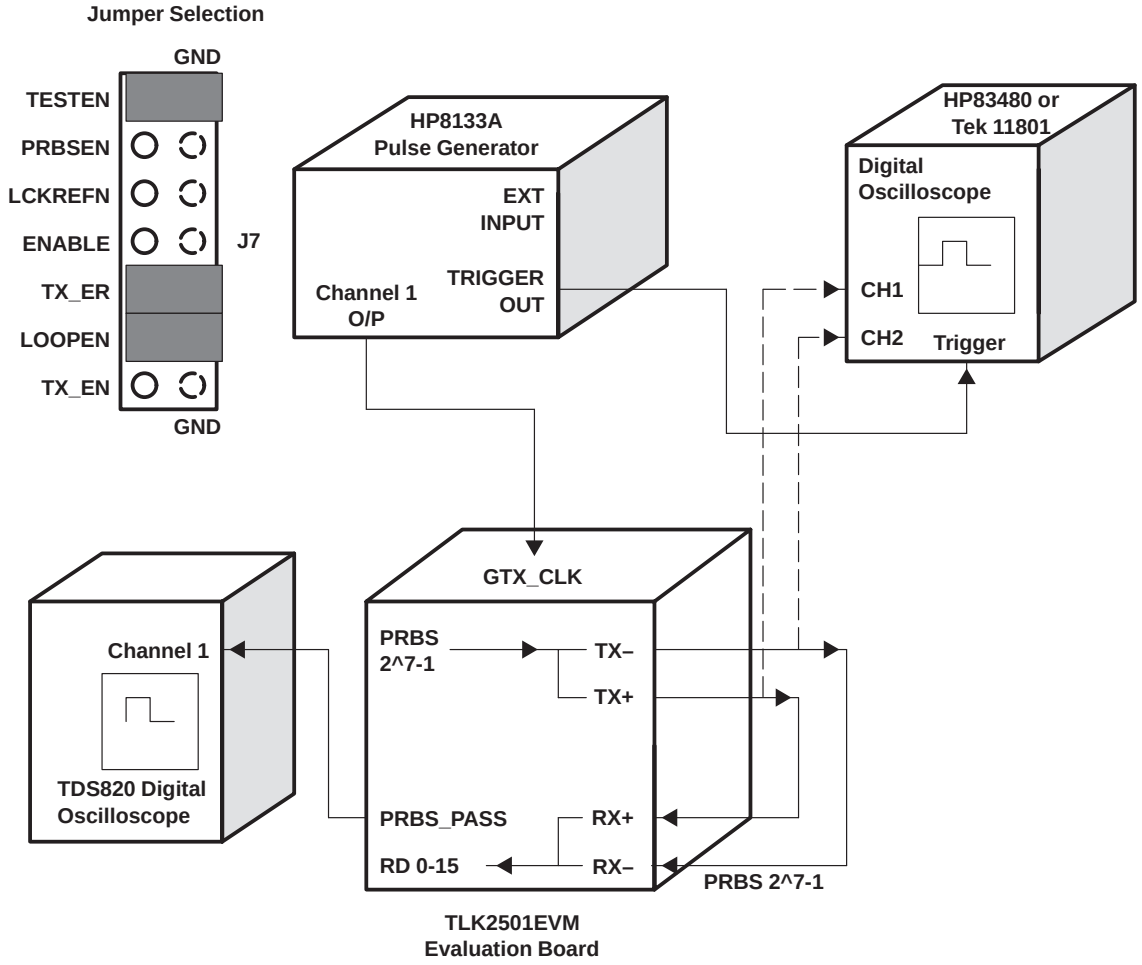
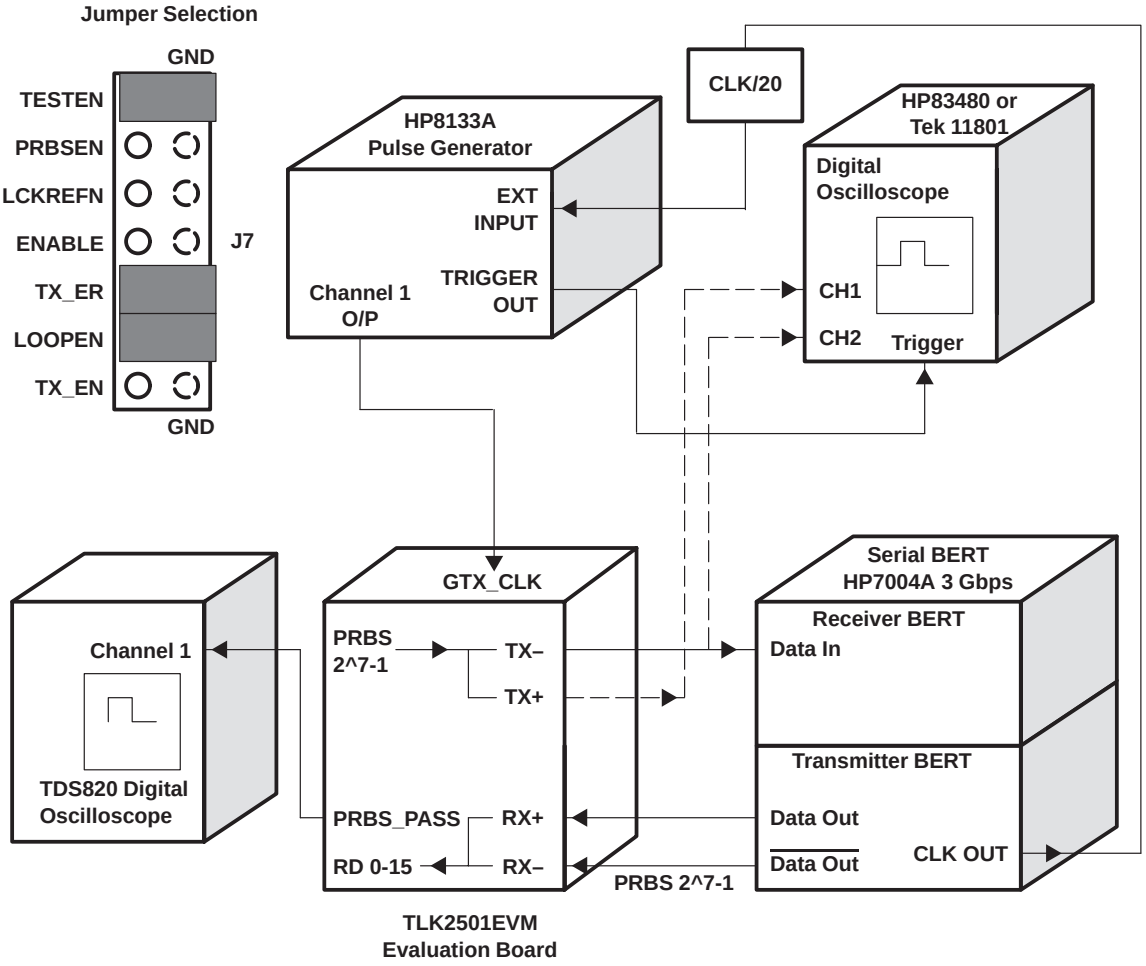
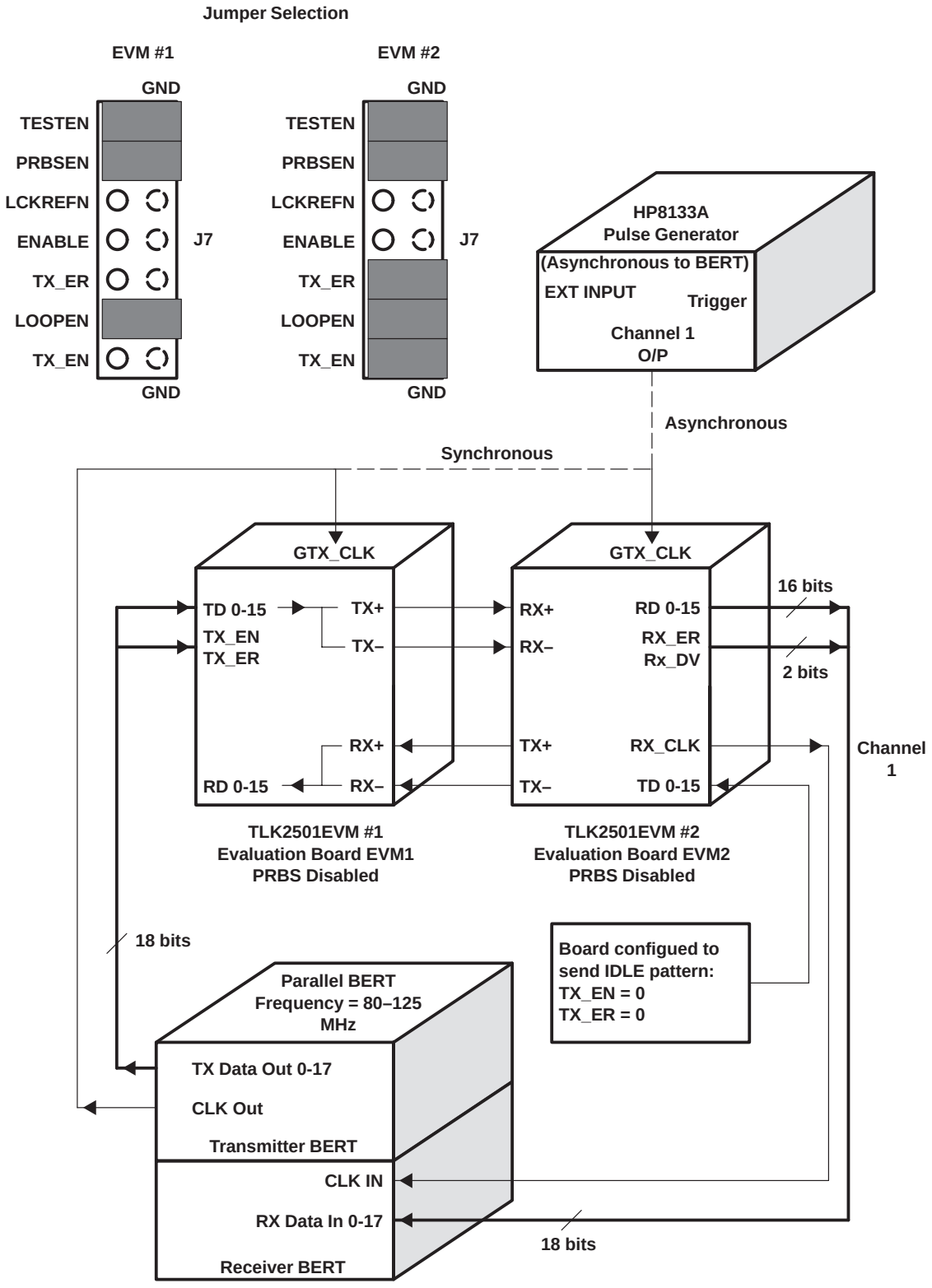


Figure 2–3. TLK2501 Serial PRBS BERT Test Configuration



A board to board communication link is a practical method of evaluating the TLK2501 in a system like environment as shown in Figure 2–4. A Parallel BERT or a logic analyzer can be used to provide and monitor signals to and from the transceiver pairs. The BERT would need to configure the TX_ER and TX_EN signals for data transmission before any data is sent. On the receive side the RX_ER and RX_DV can monitor the device for errors. Both GTX_CLK sources must have the same frequency within 200 PPM for asynchronous operation. Synchronous operation can be achieved by using either the BERT or a synchronized pulse generator to supply both boards with GTX_CLK inputs.

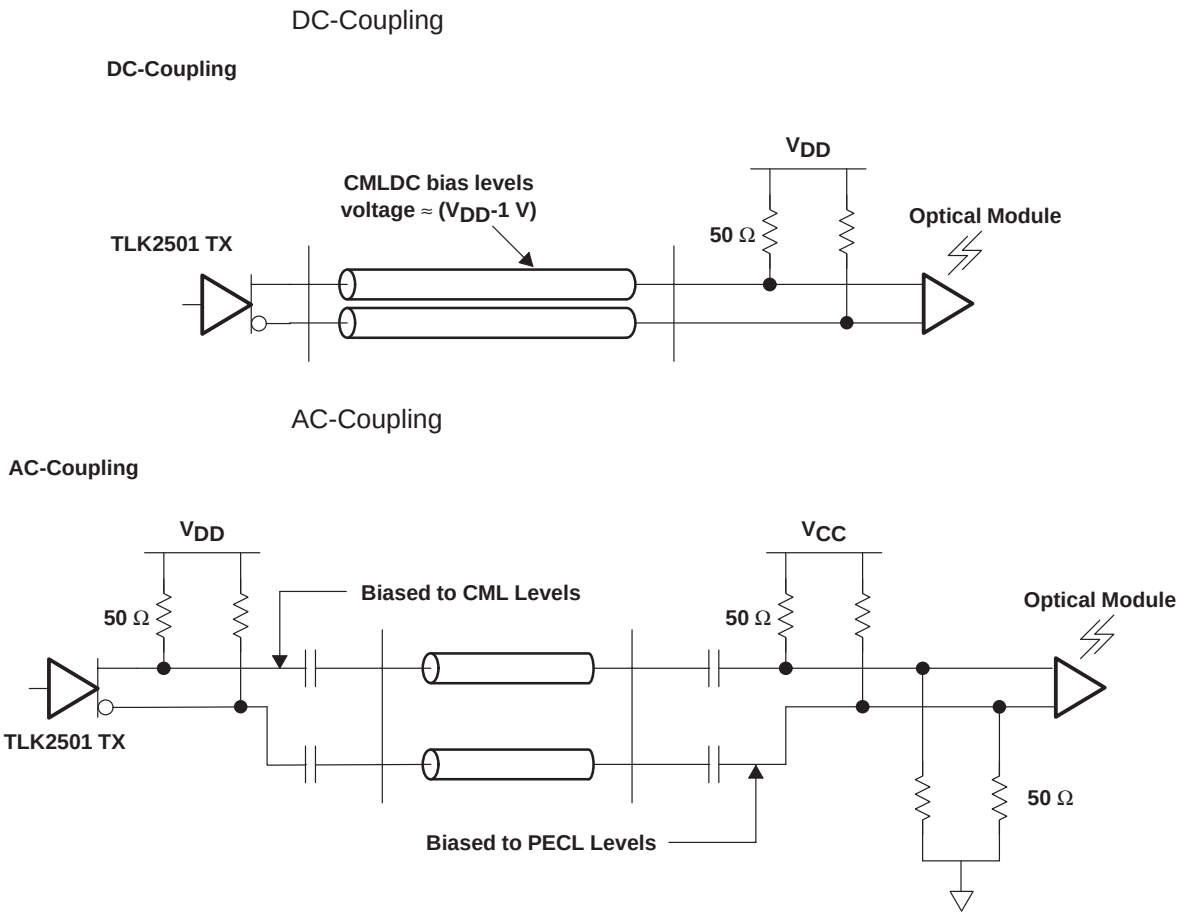
Figure 2–4. TLK2501 Serial PRBS BERT Test Configuration



2.2 Optical Interfacing and Configuration

An interface between the TLK2501EVM and an optical transceiver can be achieved in many ways depending on the design of the optics module and its associated interface circuitry. Direct connection is achieved only if the optical interface supports the current mode logic levels of the TLK2501 device (VDD – 1 V). If the optics module does not support or can not be biased to the CML levels, then ac-coupling must be used. Both ac- and dc- coupling schemes are shown in Figure 2–5. The *Laser Module Section* of the EVM is configured as an ac-coupled optics module. The board is shipped with an ac-coupled output and all that is required is external loopback cabling.

Figure 2–5. Optical Interface Configuration



The *Laser Module Section* is isolated from the rest of the board and requires external loopback as shown in Figure 2–6. This makes for a versatile system where the laser can be connected independently to other EVM systems.

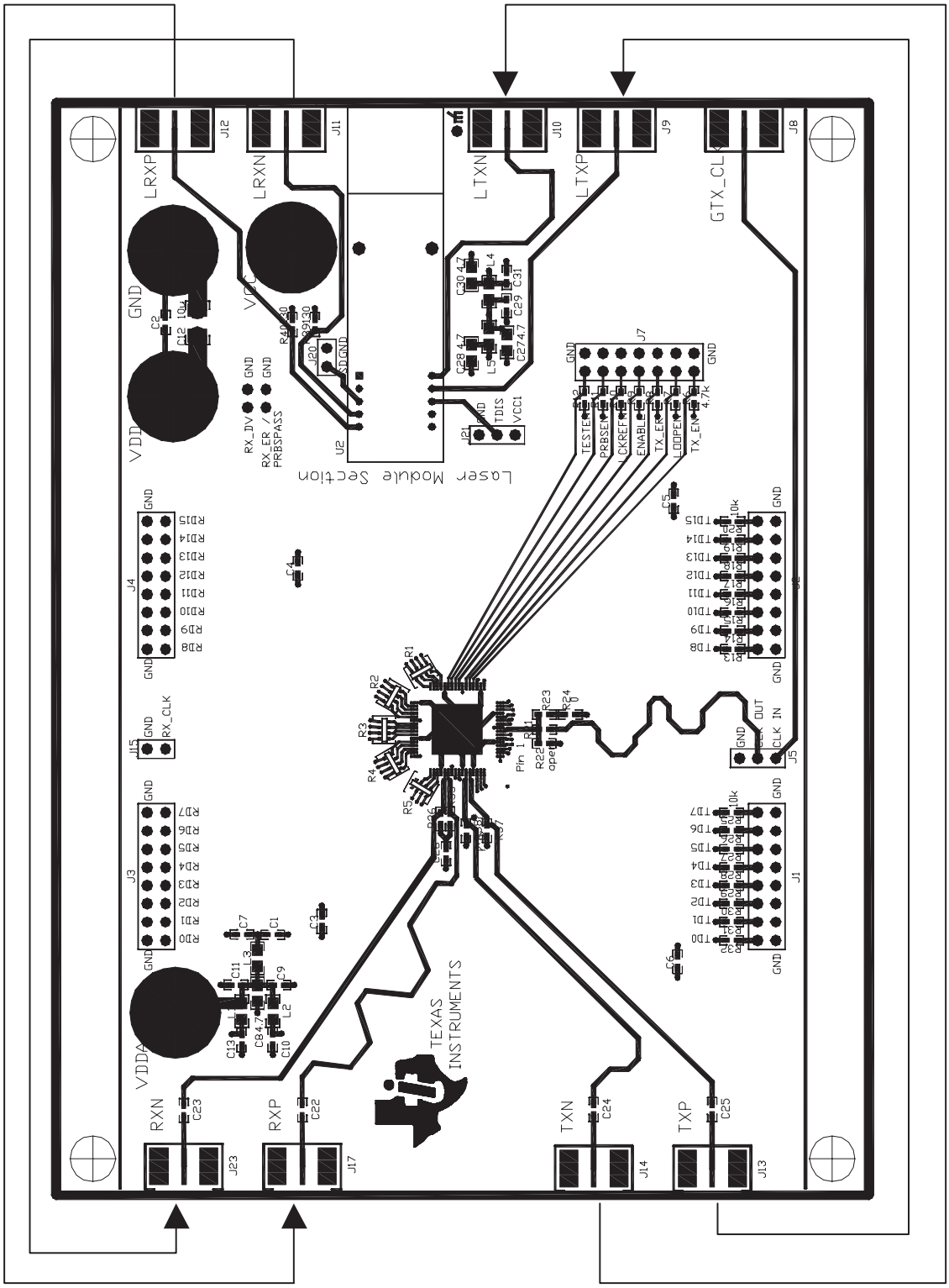


Figure 2–6. TLK2501EVM to Laser Module Configuration

Chapter 3

PCB Construction and Characteristics

The PCB characteristics are calculated and based on the layer construction and trace width of the board. This should be useful in determining the proper interface to the EVM and establishing system timing.

Table 3–1. TLK2501 EVM TTL Bus PCB Transmission Line Characteristics

Device Pin No./Des.	Connector Pin Label	Trace Width (inches)	Length (inches)	Capacitance (pF)	Inductance (nH)	Impedance (Ω)	Line Delay (ps)
62 – TXD0	TD0	0.0118	1.887	5.2	14.1	51.9	272.1
63 – TXD1	TD1	0.0118	1.884	5.2	14.1	51.9	271.7
64 – TXD2	TD2	0.0118	1.904	5.3	14.3	51.9	274.7
2 – TXD3	TD3	0.0118	1.898	5.3	14.2	51.9	273.7
3 – TXD4	TD4	0.0118	1.903	5.3	14.2	51.9	274.4
4 – TXD5	TD5	0.0118	1.899	5.3	14.2	51.9	273.8
6 – TXD6	TD6	0.0118	1.901	5.3	14.2	51.9	274.1
7 – TXD7	TD7	0.0118	1.906	5.3	14.3	51.9	274.8
10 – TXD8	TD8	0.0118	1.860	5.2	13.9	51.9	268.2
11 – TXD9	TD9	0.0118	1.908	5.3	14.3	51.9	275.1
12 – TXD10	TD10	0.0118	1.884	5.2	14.1	51.9	271.7
14 – TXD11	TD11	0.0118	1.912	5.3	14.3	51.9	275.7
15 – TXD12	TD12	0.0118	1.903	5.3	14.2	51.9	274.4
16 – TXD13	TD13	0.0118	1.910	5.3	14.3	51.9	275.4
17 – TXD14	TD14	0.0118	1.911	5.3	14.3	51.9	275.6
19 – TXD15	TD15	0.0118	1.901	5.3	14.2	51.9	274.1
51 – RXD0	RD0	0.0118	1.814	5.0	13.6	51.9	26.6
50 – RXD1	RD1	0.0118	1.804	5.0	13.5	51.9	260.3
49 – RXD2	RD2	0.0118	1.802	5.0	13.5	51.9	259.9
47 – RXD3	RD3	0.0118	1.862	5.2	13.9	51.9	268.5
46 – RXD4	RD4	0.0118	1.866	5.2	14.0	51.9	269.1
45 – RXD5	RD5	0.0118	1.876	5.2	14.0	51.9	270.5
44 – RXD6	RD6	0.0118	1.880	5.2	14.1	51.9	271.1
42 – RXD7	RD7	0.0118	1.865	5.2	14.0	51.9	268.9
40 – RXD8	RD8	0.0118	1.860	5.2	13.9	51.9	268.2
39 – RXD9	RD9	0.0118	1.860	5.2	13.9	51.9	268.2
37 – RXD10	RD10	0.0118	1.863	5.2	13.9	51.9	268.6
36 – RXD11	RD11	0.0118	1.872	5.2	14.0	51.9	269.9
35 – RXD12	RD12	0.0118	1.816	5.0	13.6	51.9	261.9
34 – RXD13	RD13	0.0118	1.855	5.2	13.9	51.9	267.5
32 – RXD14	RD14	0.0118	1.809	5.0	13.9	51.9	260.9
31 – RXD15	RD15	0.0118	1.821	5.1	13.6	51.9	262.9

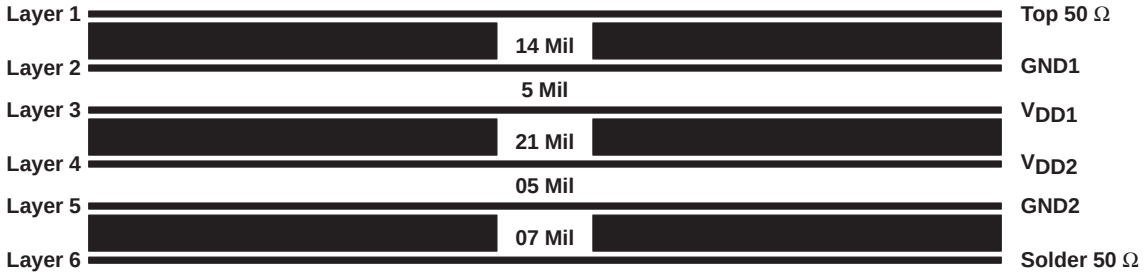
Note: All values presented in this table are theoretical calculated values and may not reflect actual measured parameters.

Table 3–2. TLK2501 Differential Pair PCB Transmission Line Characteristics

Device Pin No.	Connector Pin No.	Trace Width (inches)	Length (inches)	Impedance (Ω)	Line Delay (ps)
60 – DOUTTXP	TXP	0.025	2.390	51.2	347.5
59 – DOUTTXN	TXP	0.025	2.363	51.2	343.6
54 – DINRXP	RXP	0.025	2.889	51.2	420.1
53 – DINRXN	RXN	0.025	2.883	51.2	419.2

Note: All values presented in this table are theoretical calculated values and may not reflect actual measured parameters.

Figure 3–1. TLK2501 EVM Layer Construction



Notes:
1) All cores consist of 1 oz. Cu.
2) Trace width
A) 25 mils (for 50 Ω Layer 1)
B) 11.8 mils (for 50 Ω Layer 6)
3) Overall board thickness is 62 mils ±5 mil
4) Copper and solder mask adds approximately 10 mils to the overall board thickness.
5) Impedance is 50 Ω ±5%
6) Material is G-Tek. Dielectric constant = 3.9
7) For overall thickness: add 1.2 to 1.4 mils for each metal layer in the stack-up.

Appendix A

Schematics, Board Layouts, and Suggested Optics and Cable Assembly Specifications

This appendix contains schematics and corresponding bill of materials for the TLK2501EVM transceiver board along with board layouts. Specifications for the NetLight™ 1417K4A 1300 nm laser assembly are also included.

Figure A–1. TLK2501 EVM Transceiver Schematic

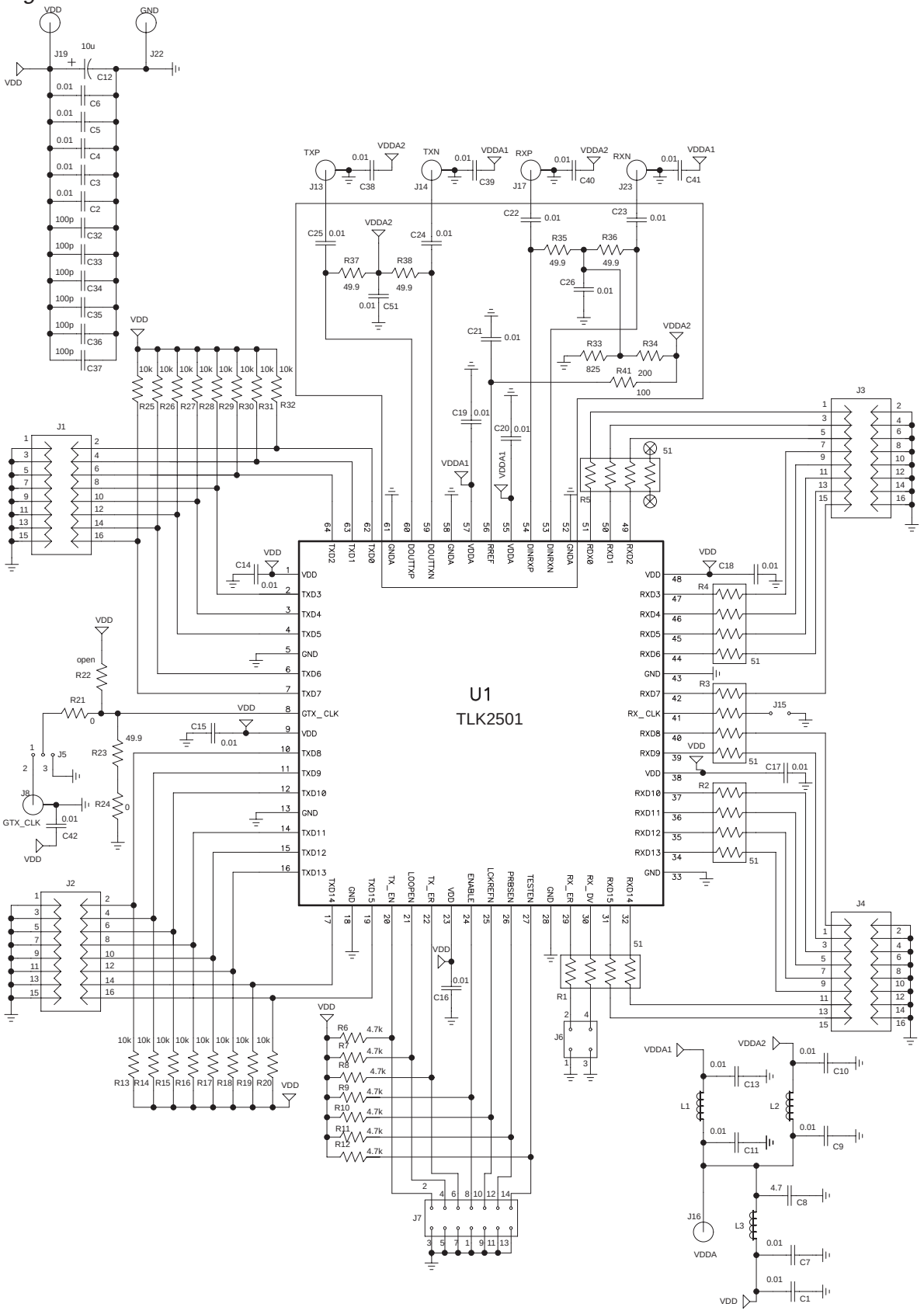


Figure A–2. Optical Transceiver Schematic

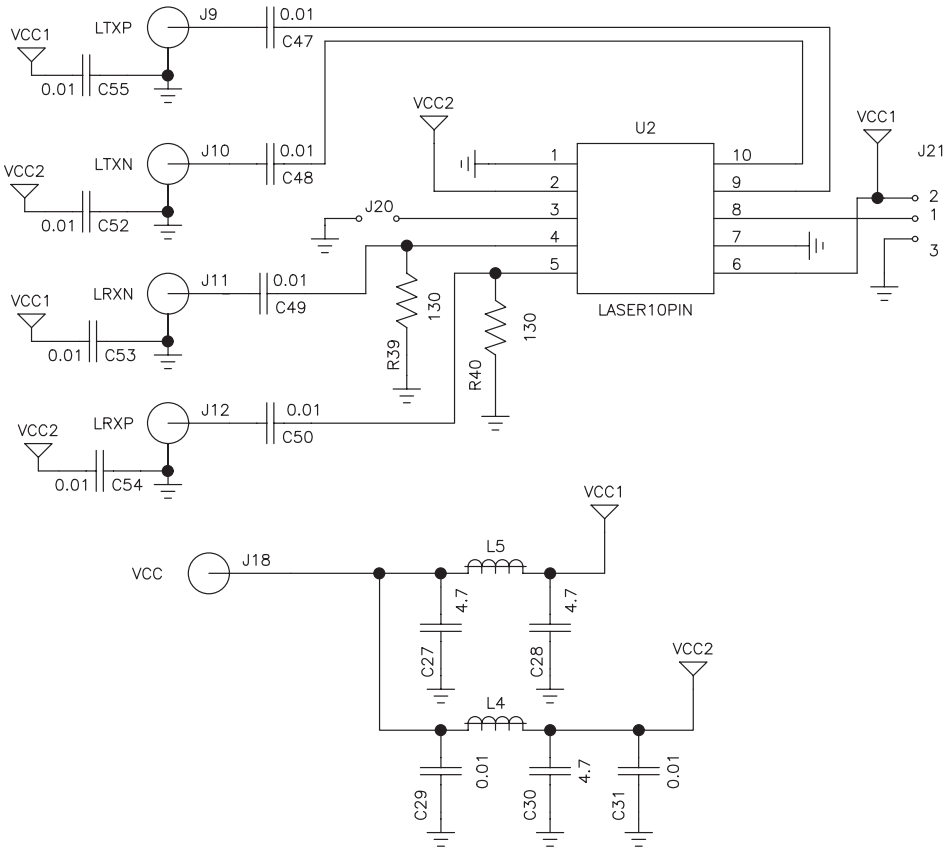


Table A–1. TLK2501 EVM Transceiver Bill of Materials

Item	Qty	Mfg / Dist.	Mfg Part No.	Ref Des	Description	Value or Function
1	1	Digi-Key	S2011–02–ND	J6	2×2 header	0.1 x 0.1 centers
2	1	Digi-Key	S2011–07–ND	J7	2×7 header	0.1 x 0.1 centers
3	4	Digi-Key	ECS–T1DX475R	J1, J2, J3, J4	2×8 header	0.1 x 0.1 centers
4	1	Digi-Key	S1111–03–ND	J5	3 Pin jumper	0.1 CENTERS
5	4	Newark	39N867	J16,J18,J19, J22	Banana jack	100 V, 5%, 0.1 µF
6	40	Digi-Key	PCC1784CT–ND	C1–C7, C9–C11, C13–C26, C29, C31, C38–C51	Capacitor, SMT603	25 V, 5%, 0.01 µF
7	4	Digi-Key	PCC1842CT–ND	C8,C27, C28,C30	Capacitor, SMT0603	25 V, 5%, 4.7 µF
8	1	Digi-Key	PCC1894CT–ND	C12	Capacitor, SMT0805	25 V, 5%, 10 µF
10	2	Digi-Key	S1111–02–ND	J15, J20	Jumper	Header, 1×2, 0.1 center
11	1	LUCENT	1417K4A LAS	U2	Laser transceiver	2.5 Gbps
12	2	Digi-Key	TSW–110–07–G–D	R21, R24	Resistor, SMT, 0402	0 Ω
13	7	Any	P4.75KLTC–ND	R6–R12	Resistor, SMT, 0402	4.7 kΩ
14	16	Digi-Key	P10.0KLTC–ND	R15–R20, R25–R32	Resistor, SMT, 0402	10 kΩ
15	5	Digi-Key	P49.9LCT–ND	R23, R35, R36, R37, R38	Resistor, SMT, 0402	49.9 Ω
16	2	Digi-Key	P130LTC–ND	R39, R40	Resistor, SMT, 0402	130 Ω
17	2	Digi-Key	P200LTC–ND	R34, R41	Resistor, SMT, 0402	200 Ω
18	1	Digi-Key	P825LTC–ND	R33	Resistor, SMT, 0402	825 Ω
19	1	N/A	N/A	R22	Resistor, SMT, 0402	OPEN
20	5		MNR14 E0AB J 510	R1, R2, R3, R4, R5	Resistor R–PAC(4)	51 Ω
21	9	Newark	142–0711–821		SMA end–launch	422 Ω
22	4	Newark	92N4922	STANDOFF	Standoff 0.5’ 4–40 thread	
23	4	Newark	30F082		Machine screw 4–40 × 3/8’	
24	1	TI	TLK2501	U1	TI TLK2501 DUT	64 PIN VQFP
25	6	Digi-Key	PCC101ACVCT–ND	C32–C37	Capacitor, SMT 0603	25 V, 20%, 100 pF
26	3	Digi-Key	240–1018–1ND	L1–L3	Ferrite bead 805 500 ma	600 Ω

Figure A–3. Top Layer 1

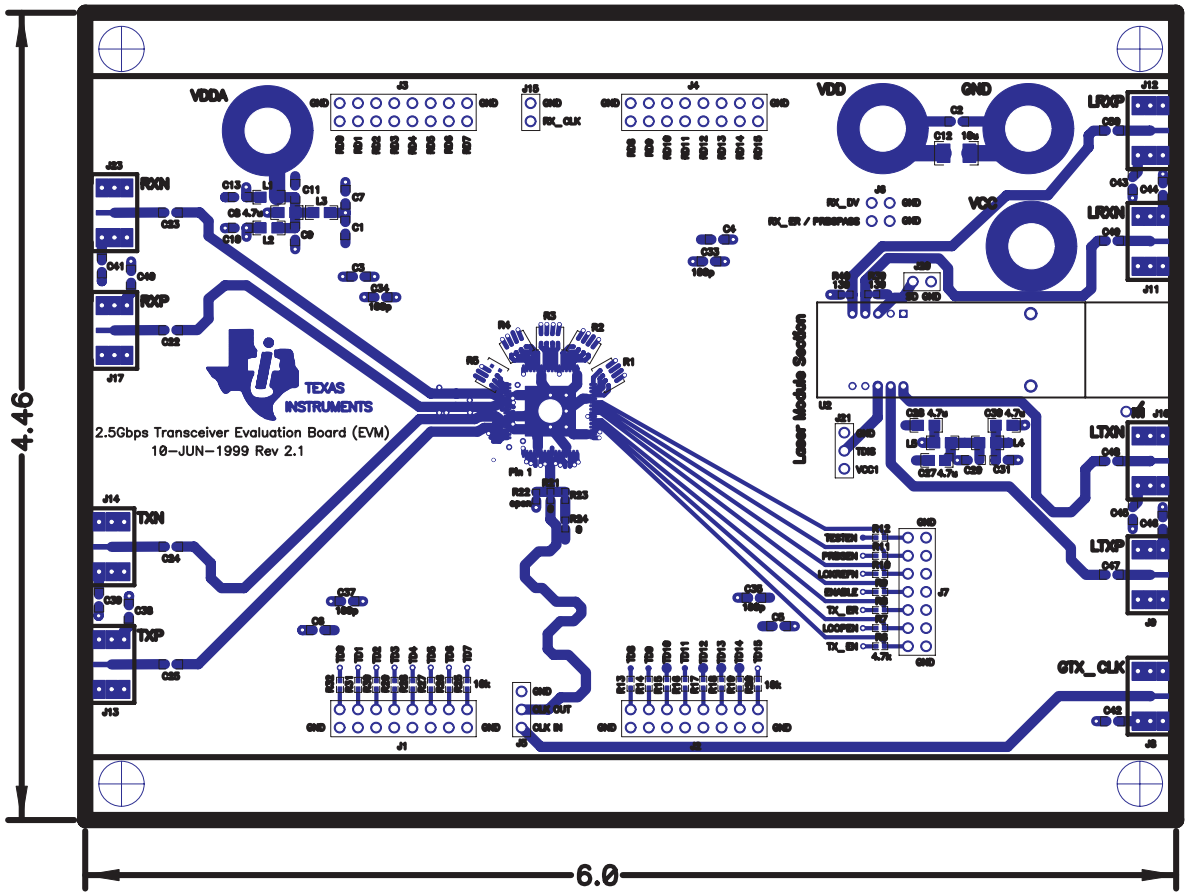


Figure A–4. GND Layers 2 and 5

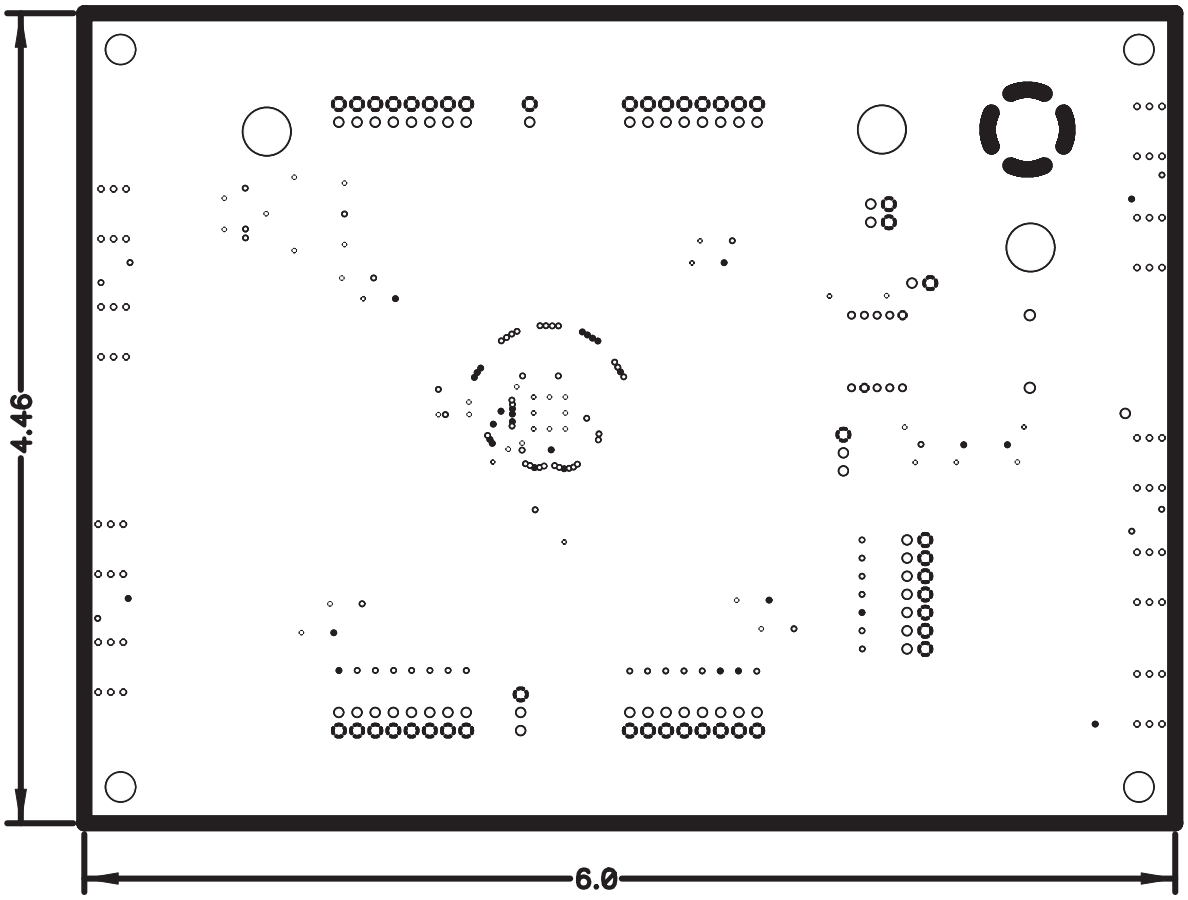


Figure A–5. Power Plane 1

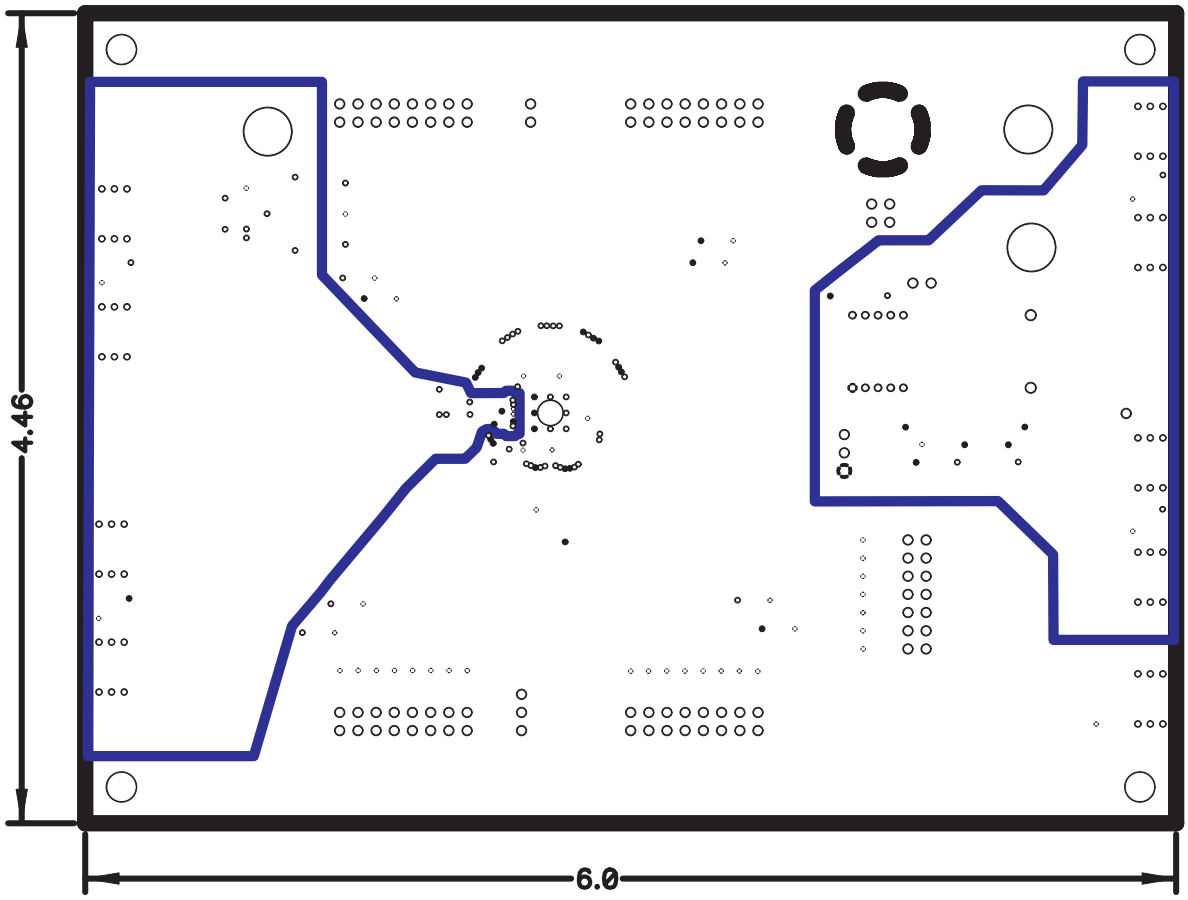


Figure A–6. Bottom Layer 6

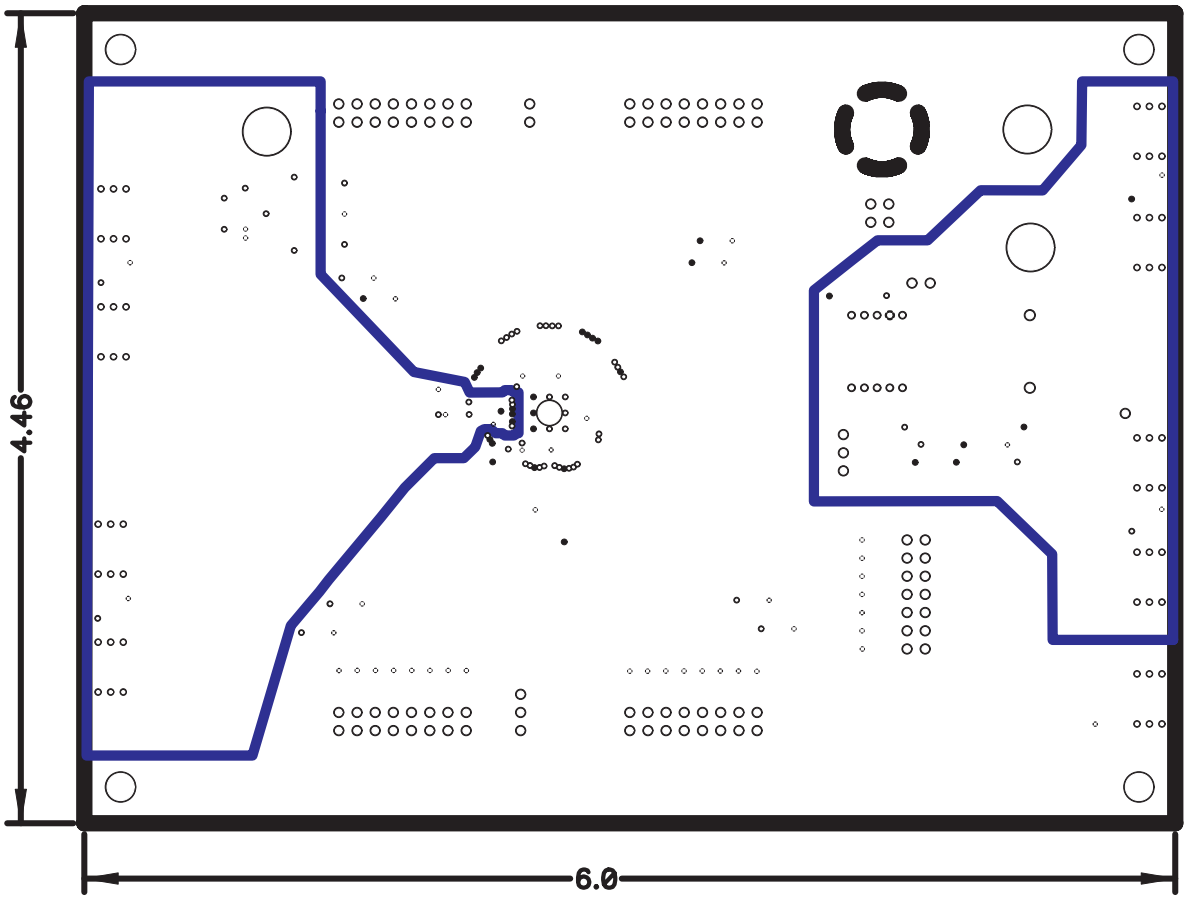
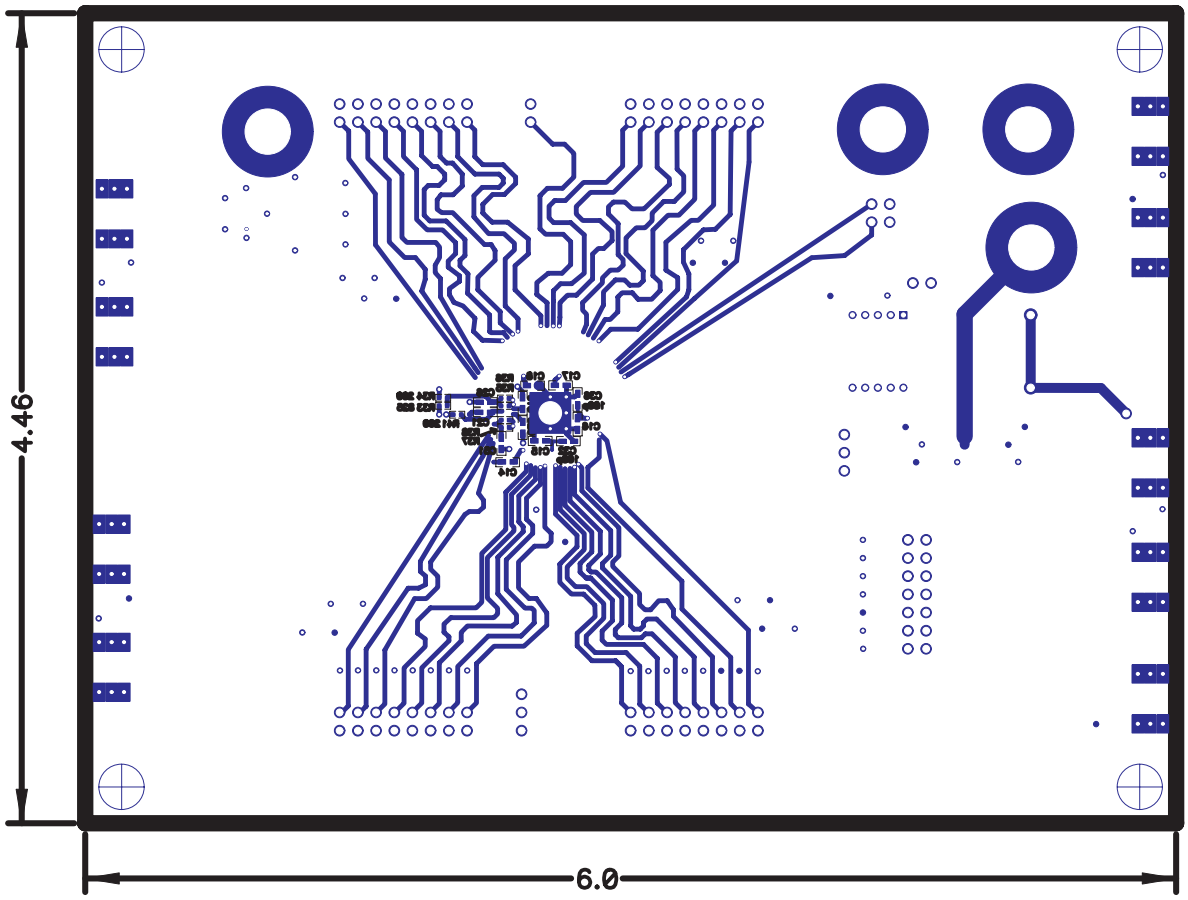


Figure A–7. Bottom Layer 7



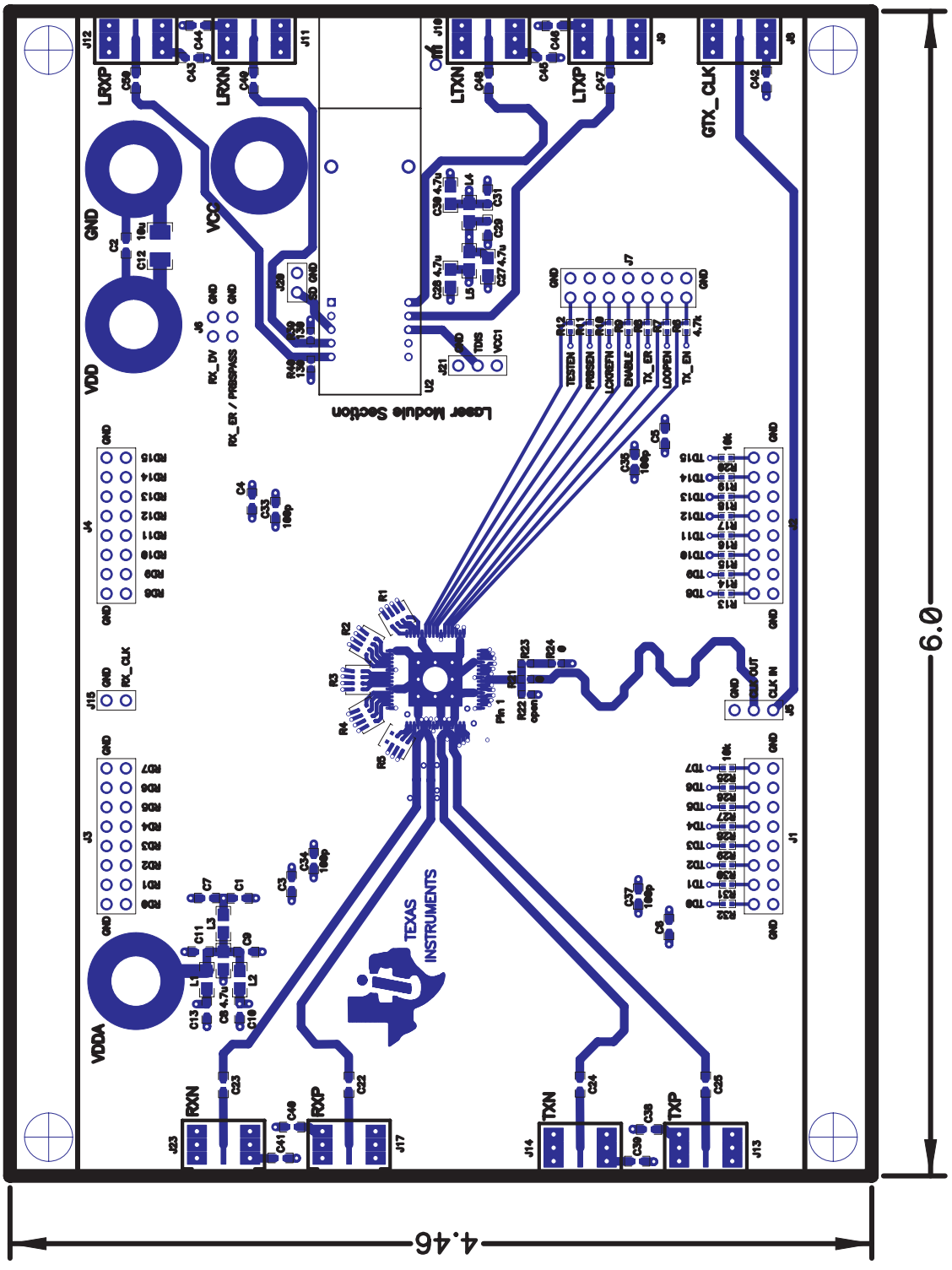


Figure A–8. Top Layer 1

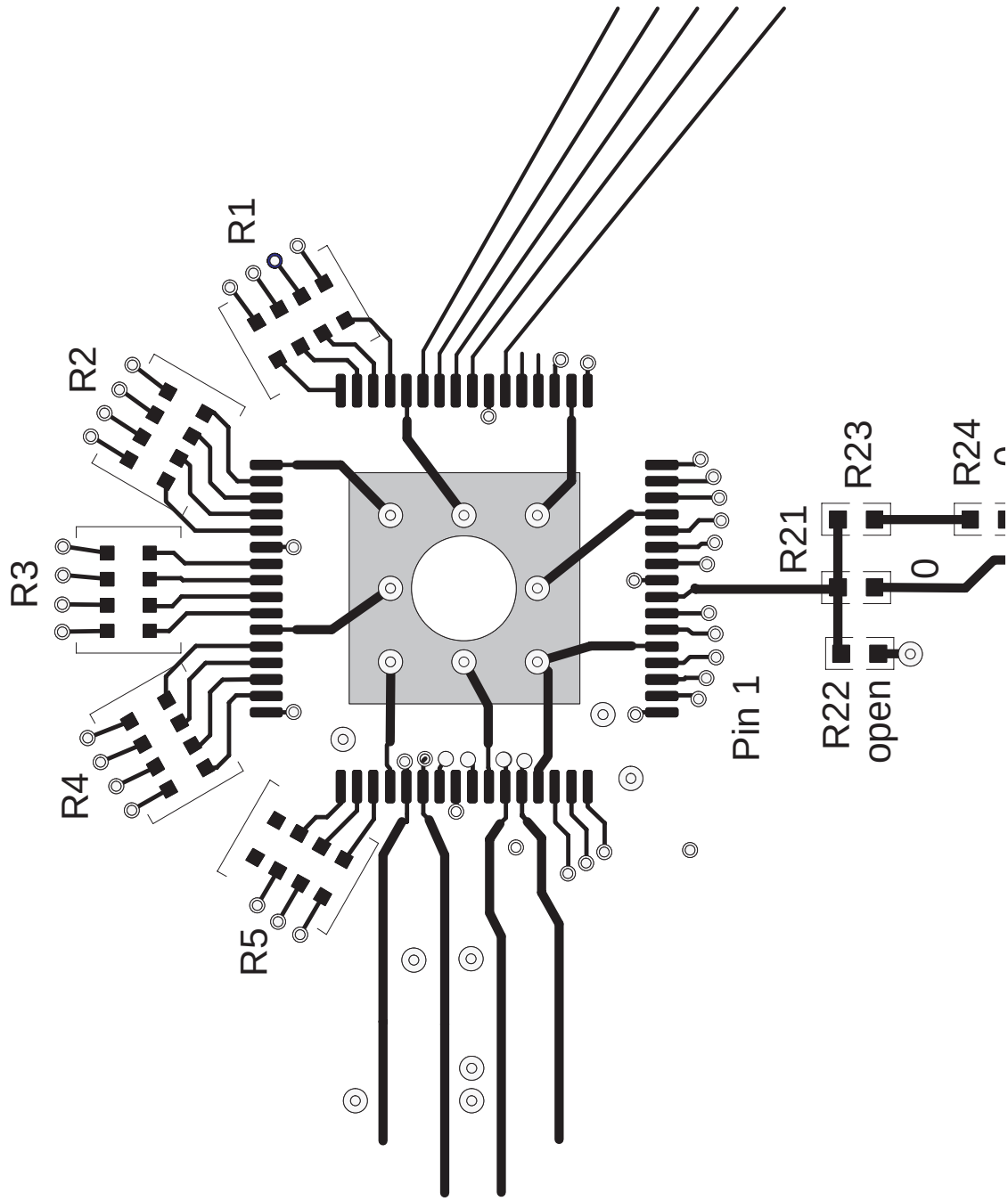


Figure A–9. Detail of Top Layer 1

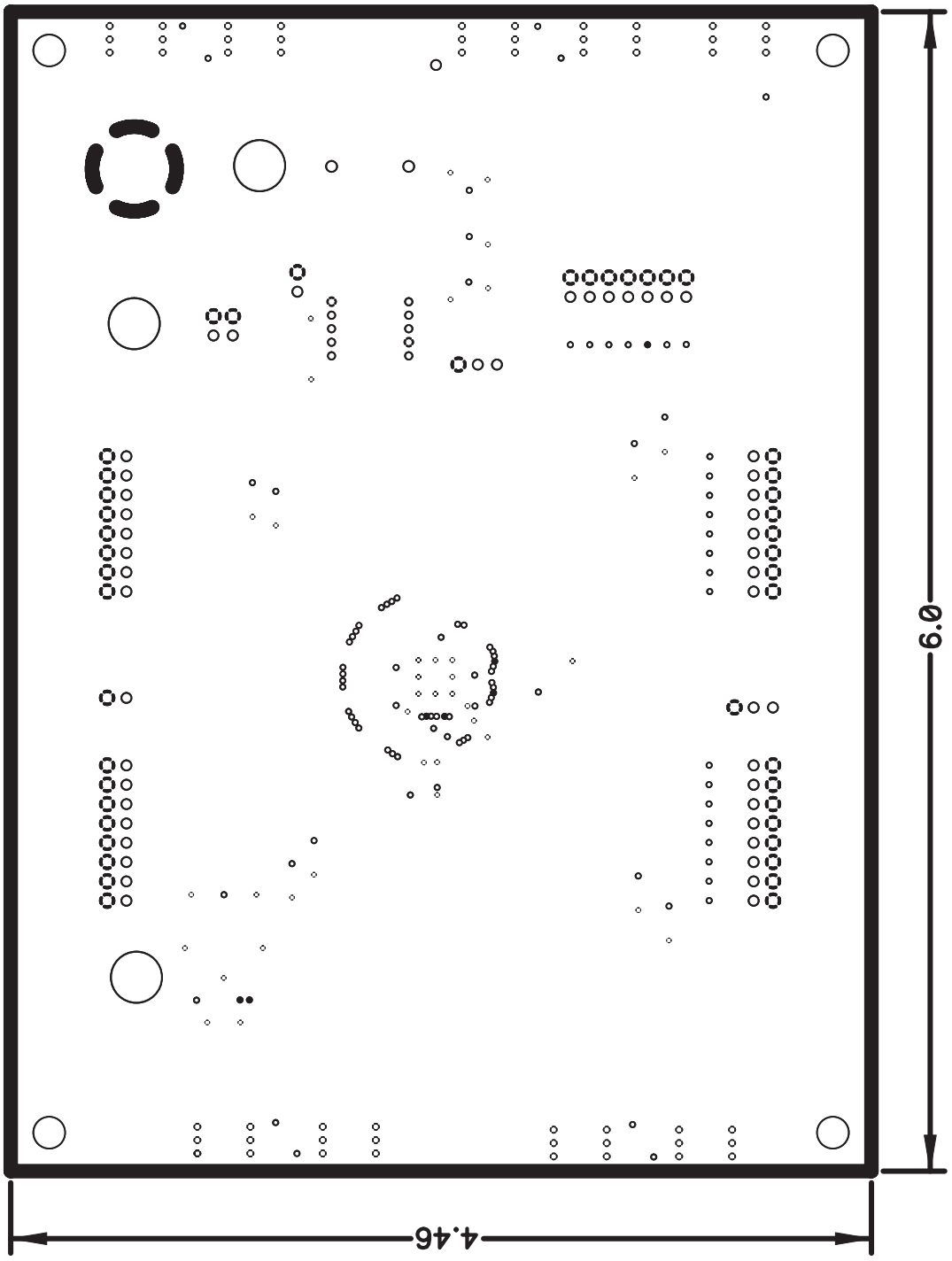


Figure A–10. GND Layers 2 and 5

Figure A–11. Detail of GND Layers 2 and 5

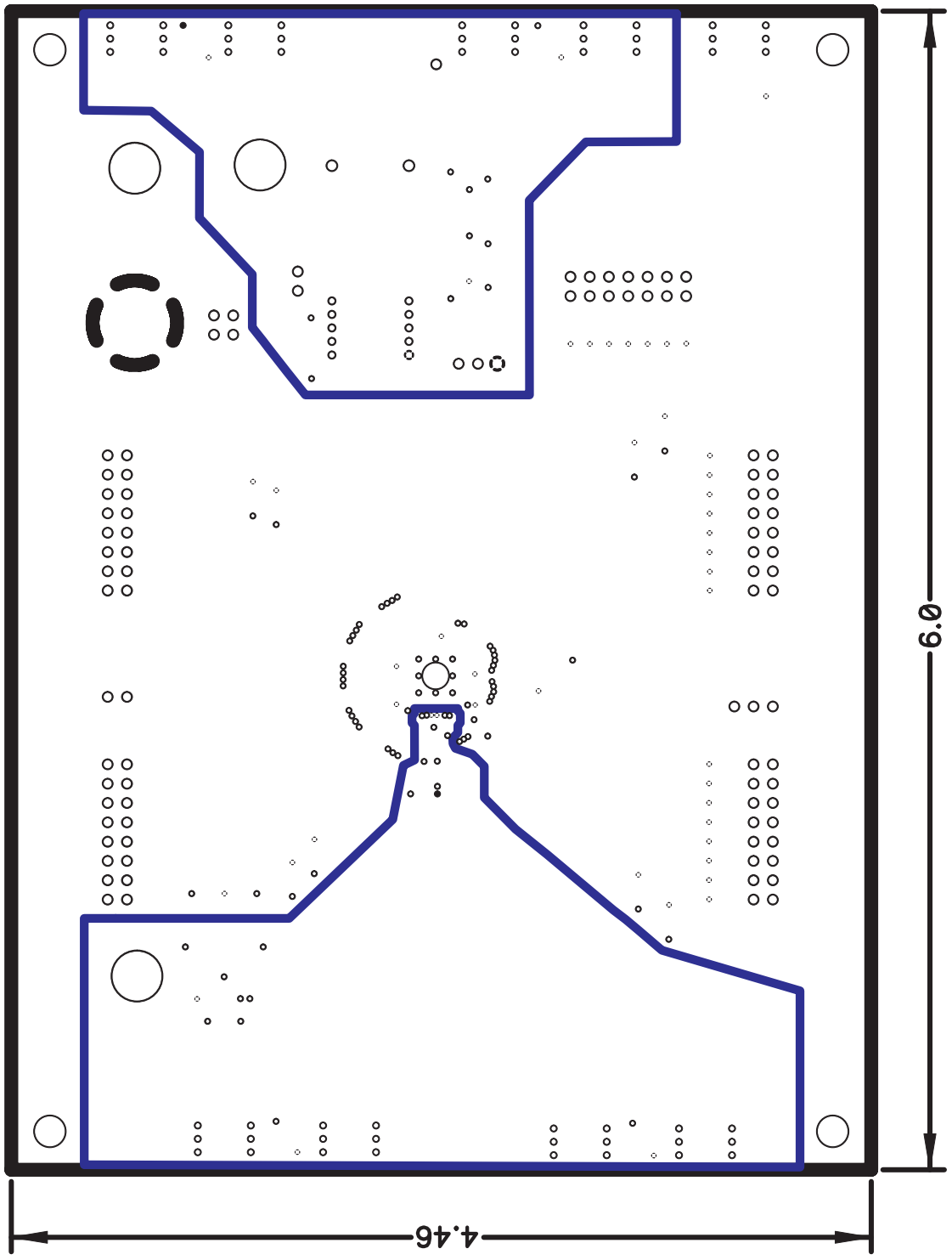


Figure A–12. Power Plane 1

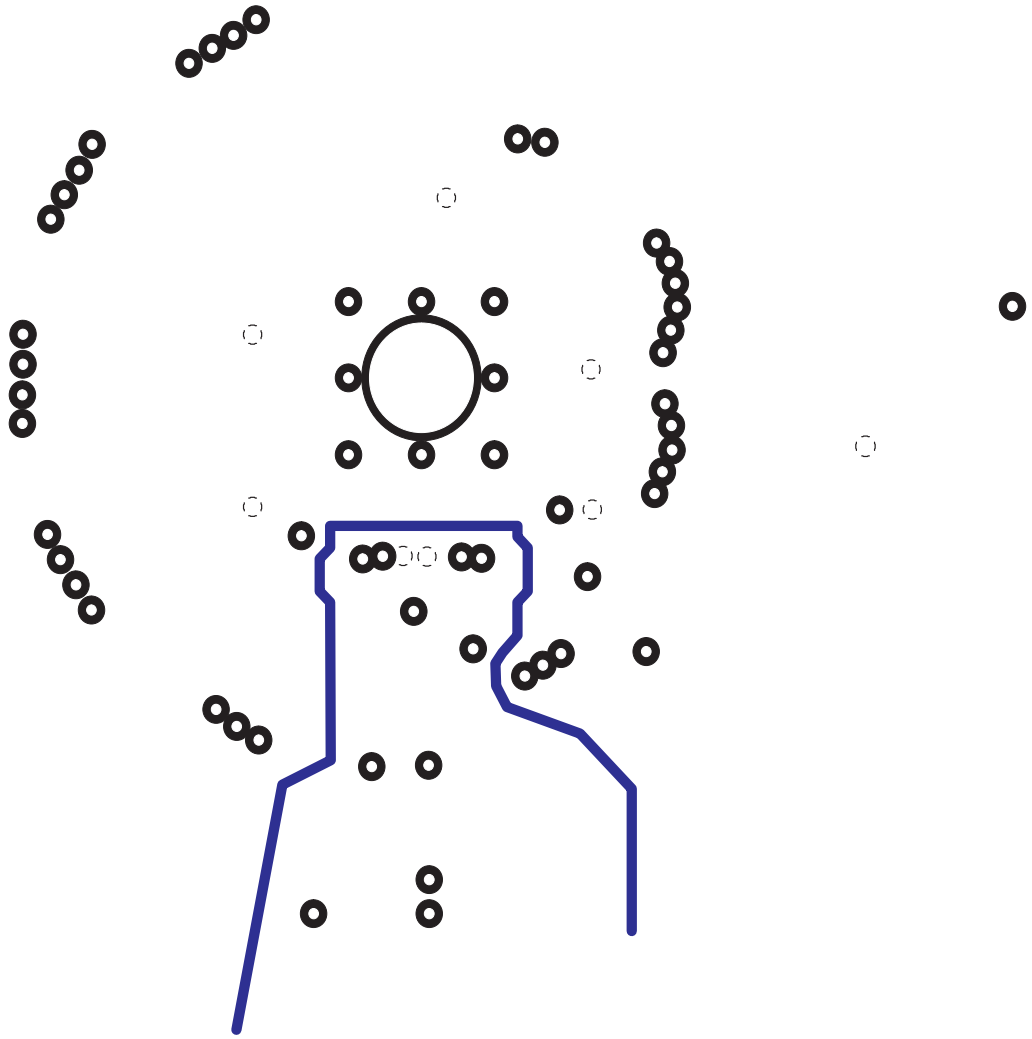


Figure A–13. Detail of Power Plane 1

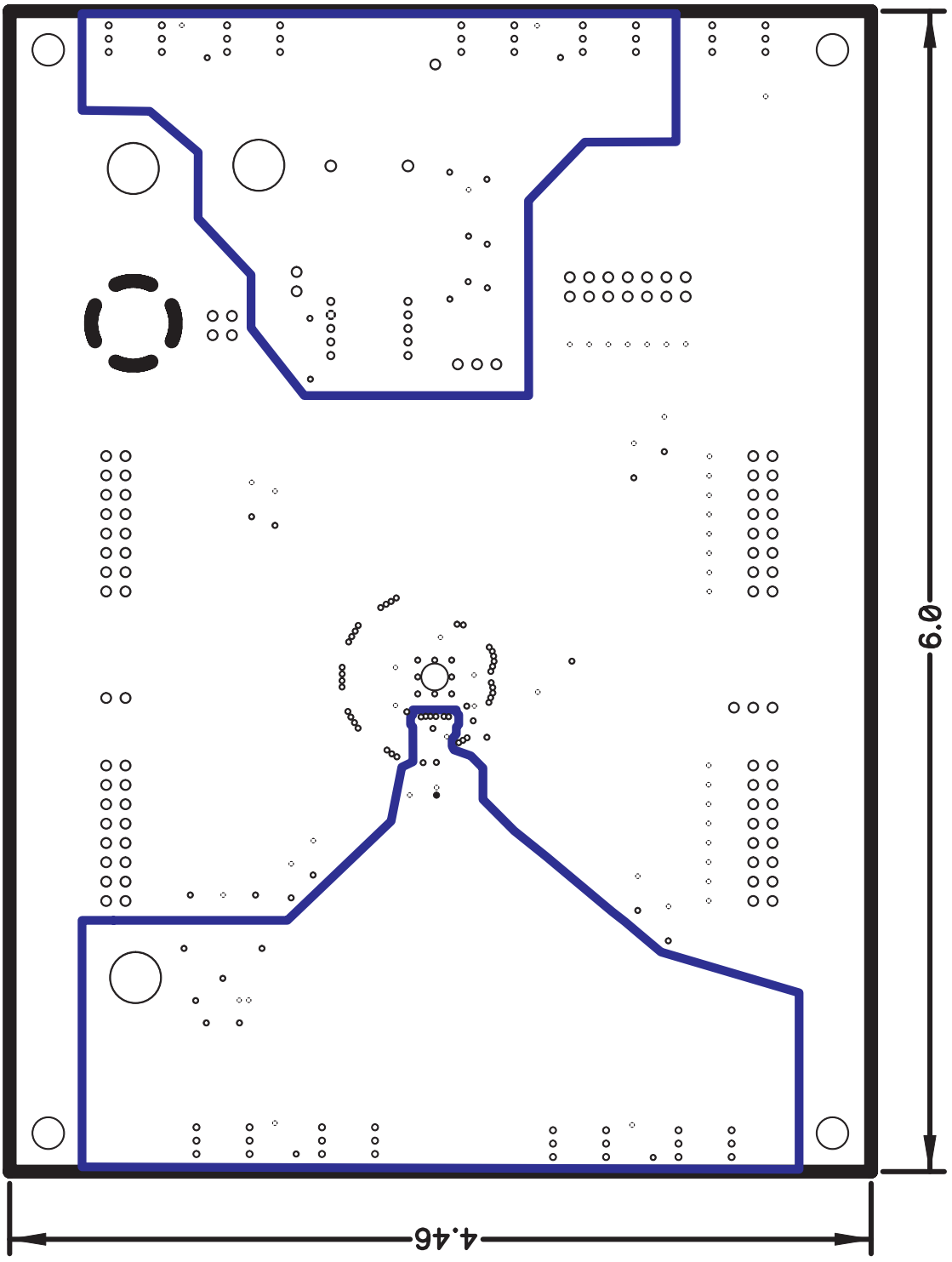


Figure A–14. Bottom Layer 6

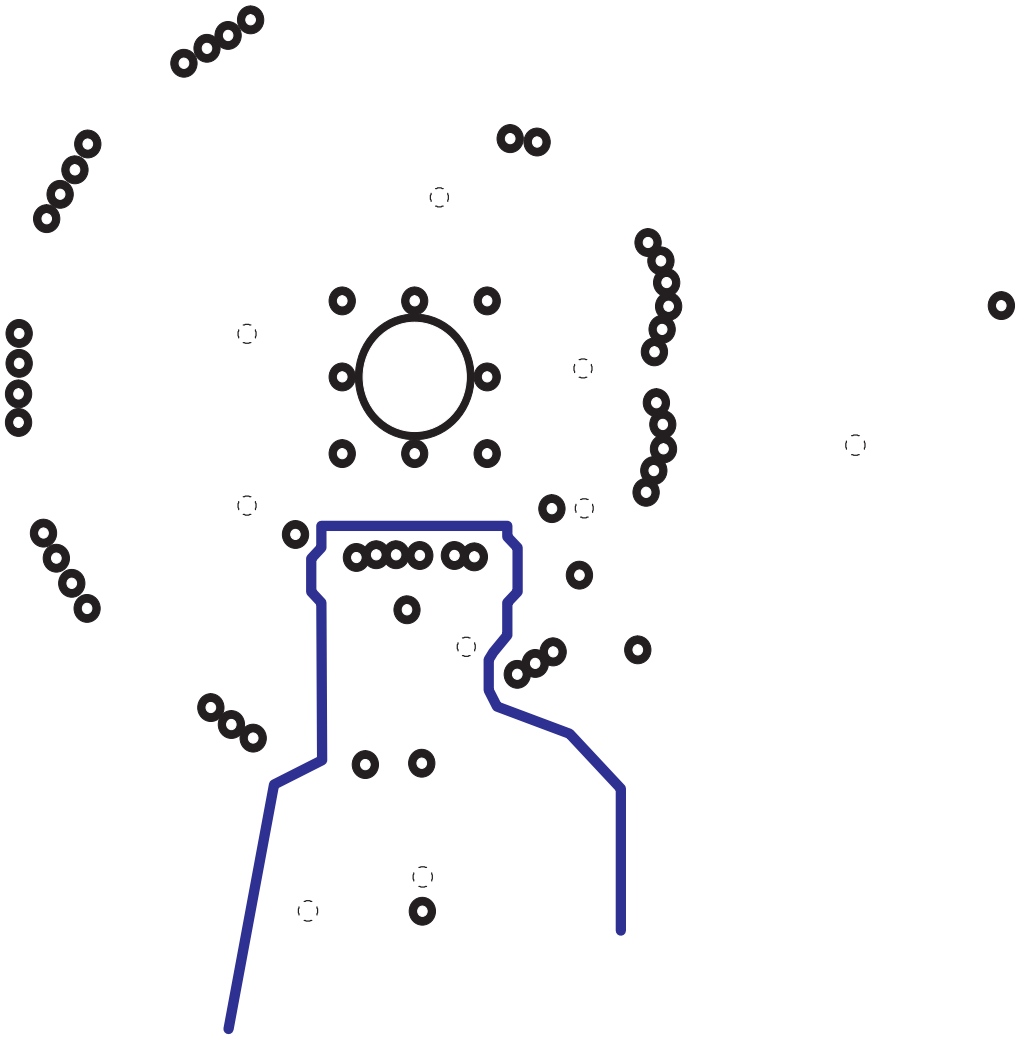


Figure A–15. Detail of Bottom Layer 6

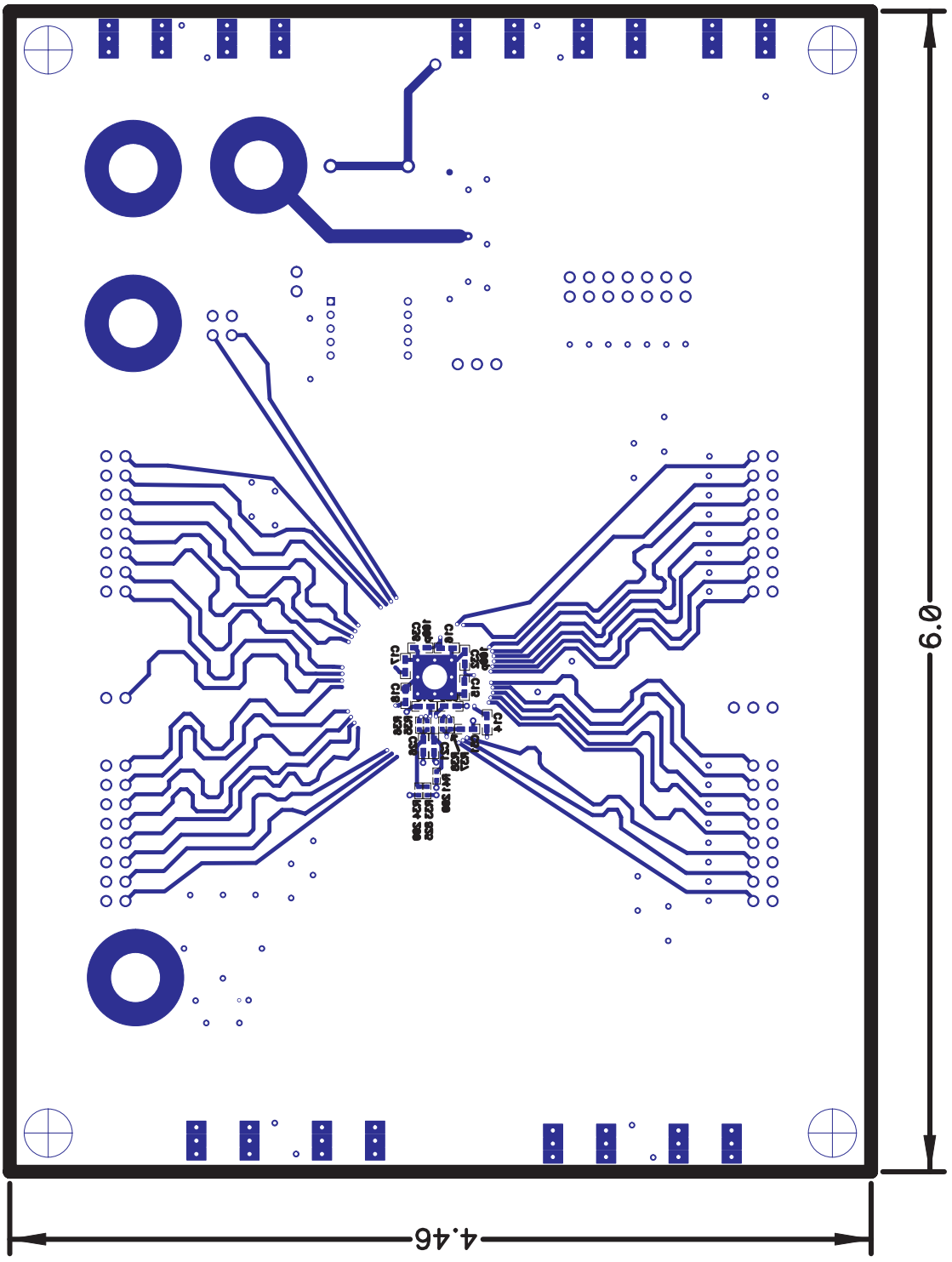


Figure A–16. Bottom Layer 6

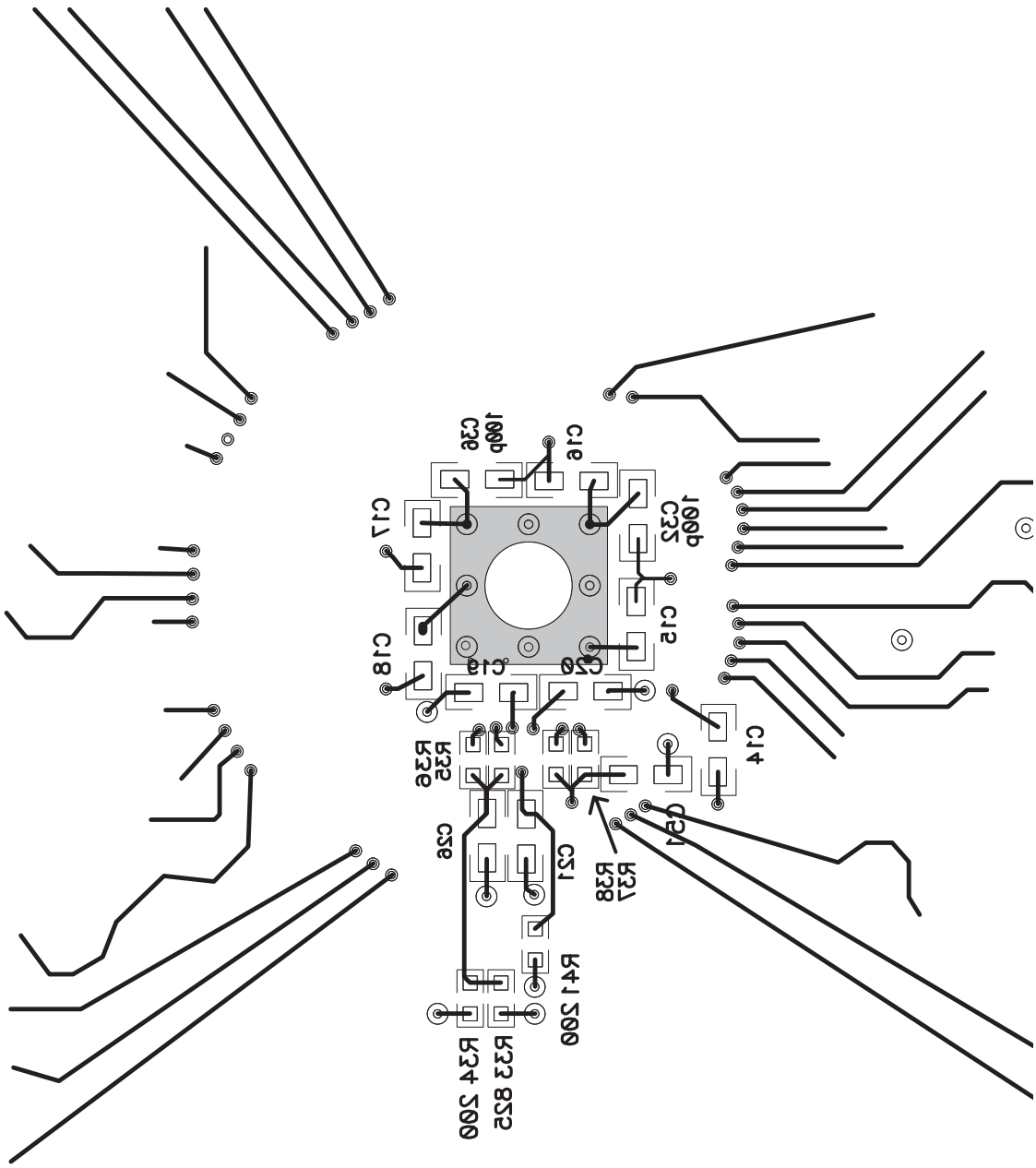


Figure A–17. Detail of Bottom Layer 6

Appendix B

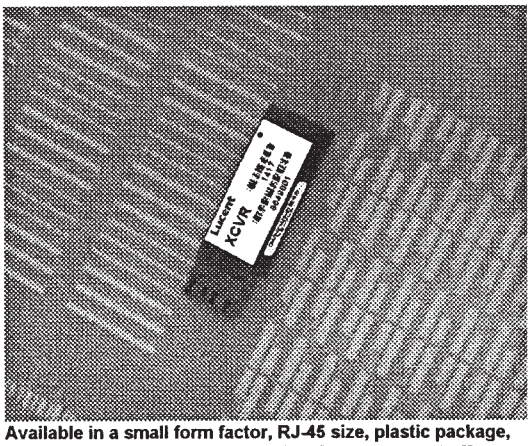
NetLight™ 1417K4A 1300 nm Laser 2.5 Gbits/s SpeedBlaster™ Transceiver

The document shown in this appendix is an advanced information data sheet from Lucent Technologies Inc.

Topic **Page**

Advanced Data Sheet
December 1999

NetLight™ 1417K4A 1300 nm 2.5 Gb/s Laser Transceiver



Available in a small form factor, RJ-45 size, plastic package, the 1417K4A Transceiver is a high-prformance, cost-effective, optical transceiver for SONET/SDH applications.

FEATURES

- SONET SR OC-48, SDH I-16 applications
- High Speed Optical Data Interface for Shelf to Shelf Interconnect
- Small Form Factor, RJ-45 size, 10-pin package
- LC duplex receptacle
- Uncooled 1300 nm laser transmitter with automatic output power control
- Transmitter disable input
- Wide dynamic range receiver with InGaAs PIN photodetector
- TTL Signal Detect output
- Low power dissipation
- Single +3.3 V power supply
- LVPECL/CML compatible data inputs and CML compatible data outputs
- Operating temperature range of 0 °C to 70 °C
- Lucent Reliability and Qualification Program for built in quality and reliability

DESCRIPTION

The 1417K4A transceiver is a high speed, cost effective optical transceiver that is intended for 2.488 Gbits/s Shelf to Shelf Optical Interconnect Applications as well as SONET SR OC-48 and SDH I-16 applications. The transceiver features the Lucent optics and is packaged in a narrow-width plastic housing with an LC duplex receptacle. This receptacle fits into an RJ-45 form factor outline. The 10-pin package pinout conforms to a multisource transceiver agreement.

The transmitter features the ability to interface to both LVPECL and CML differential logic level data inputs. The transmitter also features a TTL logic level disable input. The receiver features differential CML logic level data outputs and a TTL logic level Signal Detect output.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	0	5	V
Operating Temperature Range[1]	T_A	0	70	°C
Storage Temperature Range	T_S	-40	85	°C
Lead Soldering Temperature/Time	—	—	250/10	°C/s
Operating Wavelength Range	λ	1.1	1.6	µm

1. Under conditions of 2 m/s forced airflow.

Pin Information

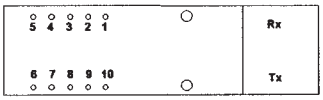


Figure 1. 1417K4A transceiver, 10-Pin Configuration, Top View

Table 1. Transceiver Pin Descriptions

Pin Number	Symbol	FUNCTIONAL DESCRIPTION	LOGIC FAMILY
		Receiver	
MS	MS	**Mounting Studs** The mounting studs are provided for transceiver mechanical attachment to the circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground.	NA
1	Vee_r	**Receiver Signal Ground**	NA
2	Vcc_r	**Receiver Power Supply**	NA
3	SD	**Signal Detect** Normal Operation: Logic one output Fault Condition: Logic zero output	LVTTL
4	RD-	**Received Data Out Bar**	CML
5	RD+	**Received Data Out**	CML
		Transmitter	
6	Vcc_t	**Transmitter Power Supply**	NA
7	Vee_t	**Transmitter Signal Ground**	NA
8	Tdis	**Transmitter Disable**	LVTTL
9	TD+	**Transmitter Data In** An internal 50 ohm termination is provided consisting of a 100 ohm resistor between the TD+ and TD- pins.	LVPECL or CML
10	TD-	**Transmitter Data In Bar** See TD+ pin for terminations.	LVPECL or CML

Electrostatic Discharge

Caution: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow EIA Standard EIA-625.

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

Lucent employs a human-body model (HBM) for ESD susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold established for the 1417K4A is ±1000 V.

Application Information

The 1417 receiver section is a highly sensitive fiber optic receiver. Although the data outputs are digital logic levels (CML), the device should be thought of as an analog component. When laying out system application boards, the 1417 transceiver should receive the same type of consideration one would give to a sensitive analog component.

Printed-Wiring Board Layout Considerations

A fiber-optic receiver employs a very high gain, wide bandwidth transimpedance amplifier. This amplifier detects and amplifies signals that are only tens of nA in amplitude when the receiver is operating near its sensitivity limit. Any unwanted signal currents that couple into the receiver circuitry cause a decrease in the receiver's sensitivity and can also degrade the performance of the receiver's signal detect (SD) circuit. To minimize the coupling of unwanted noise into the receiver, careful attention must be given to the printed wiring board.

At a minimum, a double-sided printed-wiring board (PWB) with a large component-side ground plane beneath the transceiver must be used. In applications that include many other high-speed devices, a multi-layer PWB is highly recommended. This permits the placement of power and ground on separate layers, which allows them to be isolated from the signal lines.

Multilayer construction also permits the routing of sensitive signal traces away from high-level, high-speed signal lines. To minimize the possibility of coupling noise into the receiver section, high-level, high-speed signals such as transmitter inputs and clock lines should be routed as far away as possible from the receiver pins.

Noise that couples into the receiver through the power supply pins can also degrade performance. It is recommended that the pi filter, shown in Figure 3, be used for both the transmitter and receiver power supplies.

Data and Signal Detect Outputs

Due to the high switching speeds of CML outputs, transmission line design must be used to interconnect components. To ensure optimum signal fidelity, both data outputs (RD+/RD–) should be terminated identi cally. The signal lines connecting the data outputs to the next device should be equal in length and have matched impedances. Controlled impedance stripline or microstrip construction must be used to preserve the quality of the signal into the next component and to minimize reflections back into the receiver, which could degrade its performance. Excessive ringing due to reflections caused by improperly terminated signal lines makes it difficult for the component receiving these signals to decipher the proper logic levels and can cause transitions to occur where none were intended. Also, by minimizing high-frequency ringing, possible EMI problems can be avoided.

The signal-detect output is positive LVTTL logic. A logic low at this output indicates that the optical signal into the receiver has been interrupted or that the light level has fallen below the minimum signal detect threshold. This output should not be used as an error rate indicator since its switching threshold is determined only by the magnitude of the incoming optical signal.

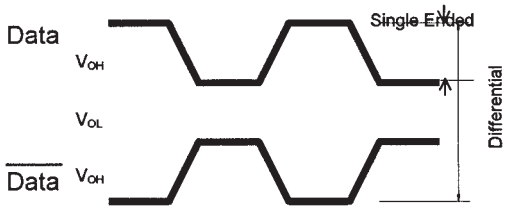


Figure 2. Data Input/Output Logic Level Definitions

Application Information (continued)

Transceiver Processing

When the process plug is placed in the transceiver's optical port, the transceiver and plug can withstand normal wave soldering and aqueous spray cleaning processes. However, the transceiver is not hermetic, and should not be subjected to immersion in cleaning solvents. The transceiver case should not be exposed to temperatures in excess of 125 °C. The transceiver pins can be wave soldered at 250 °C for up to 10 seconds. The process plug should only be used once. After removing the process plug from the transceiver, it must not be used again as a process plug; however, if it has not been contaminated, it can be reused as a dust cover.

Transceiver Optical and Electrical Characteristics

Table 2. Transmitter Optical and Electrical Characteristics (T_A = 0° C to +70° C, V_{CC} = 3.135 V - 3.465 V)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Average Optical Output Power (EOL)	P_O	-10.0	-3	dBm
Optical Wavelength	λc	1266	1360	nm
Spectral Width	$\Delta\lambda_{RMS}$	–	4	nm
Dynamic Extinction Ratio	EXT	8.2	–	dB
Rise/Fall Time (20%-80%)	T_r/T_f	–	130	ps
Power Supply Current	I_{CCT}	–	150	mA
Input Data Voltage – Single Ended[1]	$V_{IN\ p\text{-}p}$	150	800	mV p-p
Input Data Voltage – Differential[1]	$V_{IN\ p\text{-}p}$	300	1600	mV p-p
Transmit Disable Voltage[2]	V_D	Vcc-0.9	Vcc	V
Transmit Enable Voltage[2]	V_{EN}	Vee	Vee+0.8	V

Table 3. Receiver Optical and Electrical Characteristics (T_A = 0° C to +70° C, V_{CC} = 3.135 V - 3.465 V)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Average Sensitivity[3]				
800 mV (CML) Differential Input to Transmitter	P_I	–	-18	dBm
1600 mV (LVPECL) Differential Input to Transmitter	P_I	–	-16	dBm
Maximum Input Power[3]	P_{MAX}	-3	–	dBm
Power Supply Current	I_{CCR}	–	150	mA
Output Data Voltage – Single Ended[1]	$V_{IN\ p\text{-}p}$	300	500	mV p-p
Output Data Voltage – Differential[1]	$V_{IN\ p\text{-}p}$	600	1000	mV p-p
Signal Detect Switching Threshold				
Assert	LSTD	-45	-19	dBm
Deassert	LSTI	–	-18.5	dBm
Signal Detect Hysteresis	HYS	0.5	6	dB
Signal Detect Voltage[2]				
Low	V_{OL}	0.0	0.8	V
High	V_{OH}	2.4	Vcc	V
Signal Detect Response Time	SDRT		100	µs

1. 50Ω load, measured single ended. Differential operation is necessary for optimum performance. (See Figure 2 for a visual representation)
2. TTL compatible interface
3. 2^{23}-1 PRBS with a BER of 10^{-10}

Qualification and Reliability

To help ensure high product reliability and customer satisfaction, Lucent is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronic modules are qualified to Lucent internal standards as well as other appropriate industry standards using MIL-STD-883 test methods and procedures, and using sampling techniques consistent with Bellcore requirements. The 1417 Transceiver will be subjected to a set of qualification tests.

In addition, Lucent Technologies Microelectronics Group Optoelectronics Unit design, development, and manufacturing facilities have been certified to be in full compliance with the latest ISO-9001 Quality System Standards.

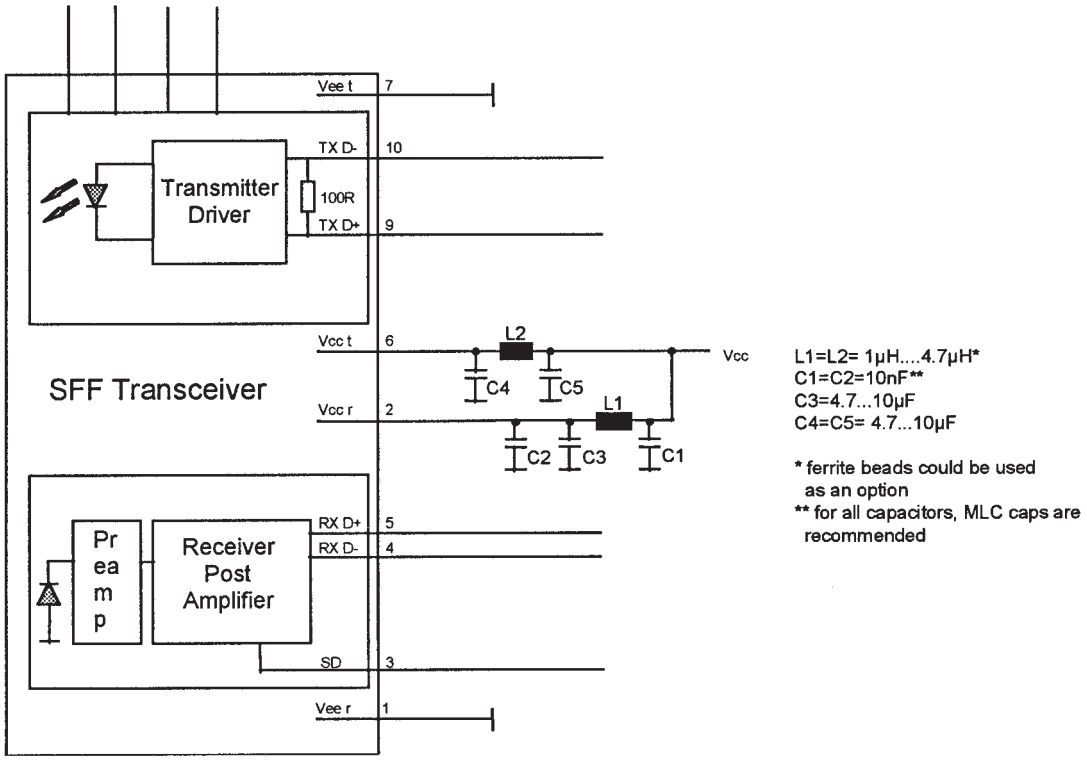
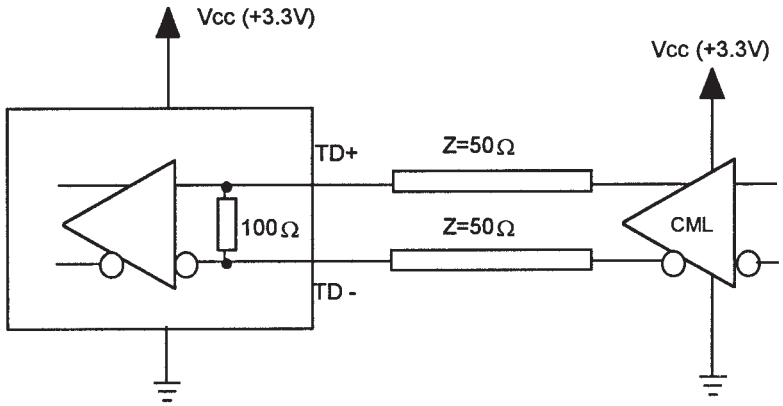
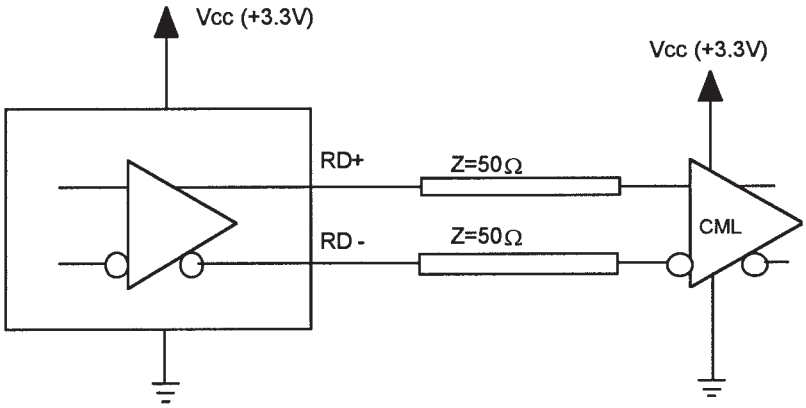


Figure 3: Power Supply Filtering of SFF transceiver

Electrical Data Interface - Current Mode Logic(CML)



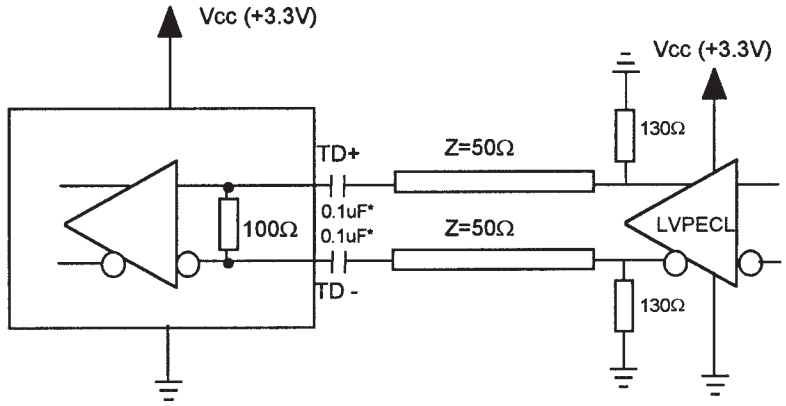
(a) Transmitter Interface – DC Coupled - (CML)



(b) Receiver Interface - DC Coupled - (CML)

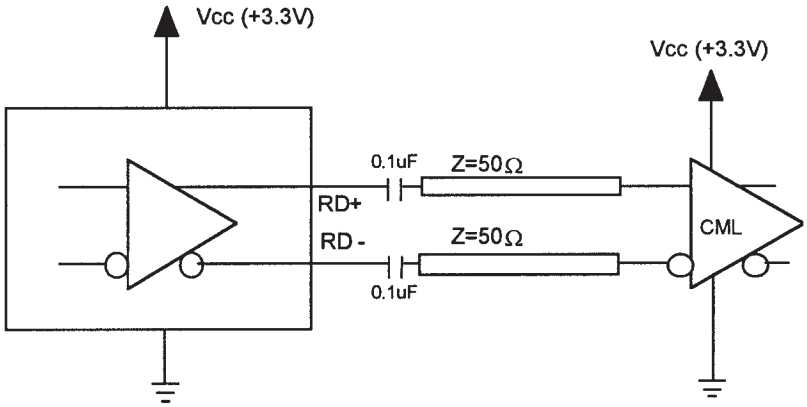
Figure 4: 3.3V Transceiver Interface with 3.3V IC's and CML

Alternate Electrical Data Interface Options



* Optional AC Coupling Capacitors - use ceramic X7R or equivalent

(a) Transmitter Interface – AC or DC Coupled - (LVPECL)

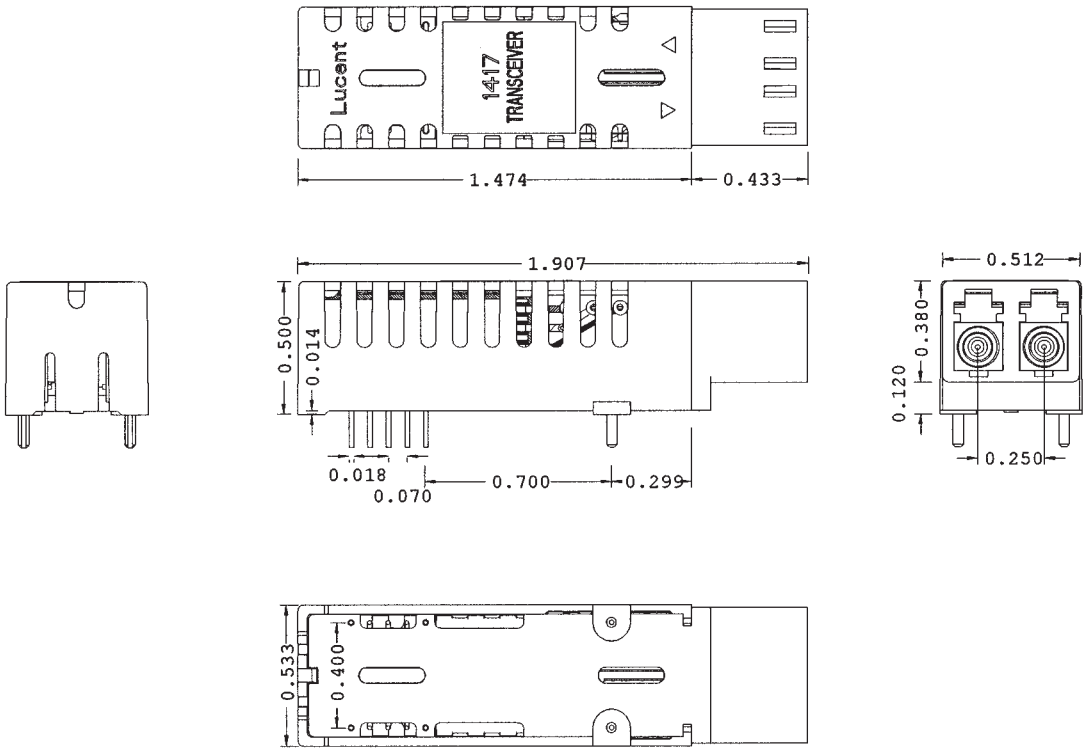


(b) Receiver Interface AC Coupled - (CML)

Figure 5: 3.3V Transceiver Interface with 3.3V IC's

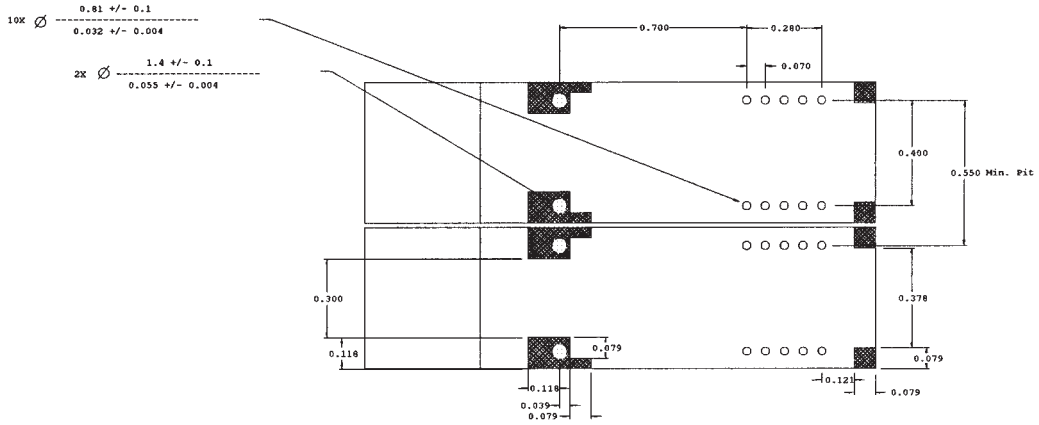
Outline Drawing

Dimensions in inches.

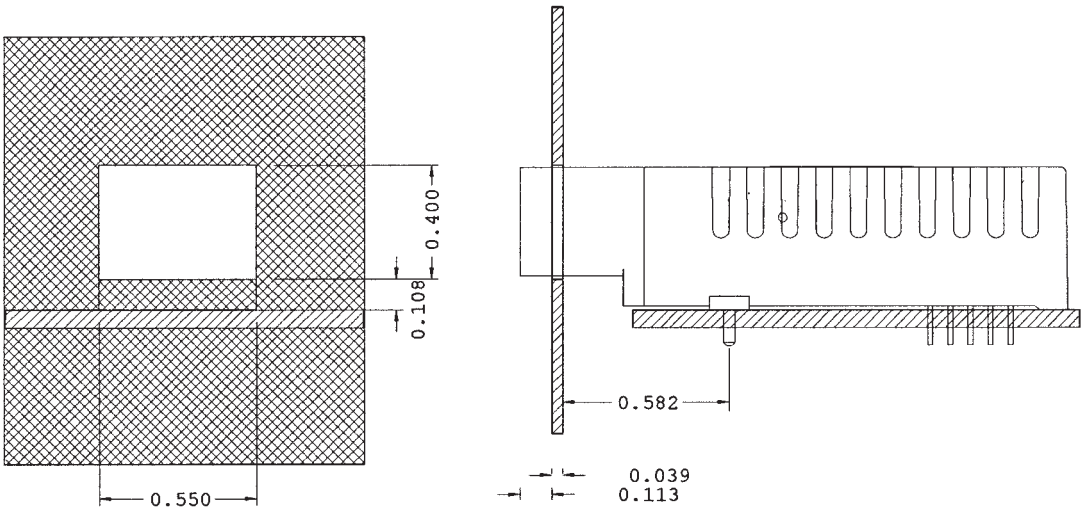


Printed Wiring Board Layout

Dimensions in inches.



Recommended Panel Opening



Laser Safety Information

Class I Laser Product

All versions of the transceiver are Class I laser products per CDRH, 21 CFR 1040 Laser Safety requirements. All versions are Class I laser products per IEC 825-1:1993. The transceiver has been certified with the FDA under accession number 8720009.

CAUTION: Use of controls, adjustments, and procedures other than those specified herein may result in hazardous laser radiation exposure.

This product complies with 21 CFR 1040.10 and 1040.11.
Wavelength = 1.3 μm
Maximum power = 1.58 mW

Product is not shipped with power supply.

NOTICE
Unterminated optical receptacles may emit laser radiation.

Do not view with optical instruments.

Ordering Information

Table 4. Ordering Information

Description	Device Code	Comcode
2 x 5 Singlemode SFF LC receptacle transceiver for 2.488 Gbits/s applications	1417K4A	108416694

NOTES:

For additional information, contact your Microelectronics Group Account Manager or the following:
OPTOELECTRONICS BUSINESS UNIT: Optoelectronics Center, 9999 Hamilton Blvd., Breinigsville, PA 18031-9359
610-391-2520, FAX 610-391-2535
INTERNET: **http://www.lucent.com/micro**
U.S.A.: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106), e-mail **docmaster@micro.lucent.com**
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
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For technical inquiries in Europe:
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